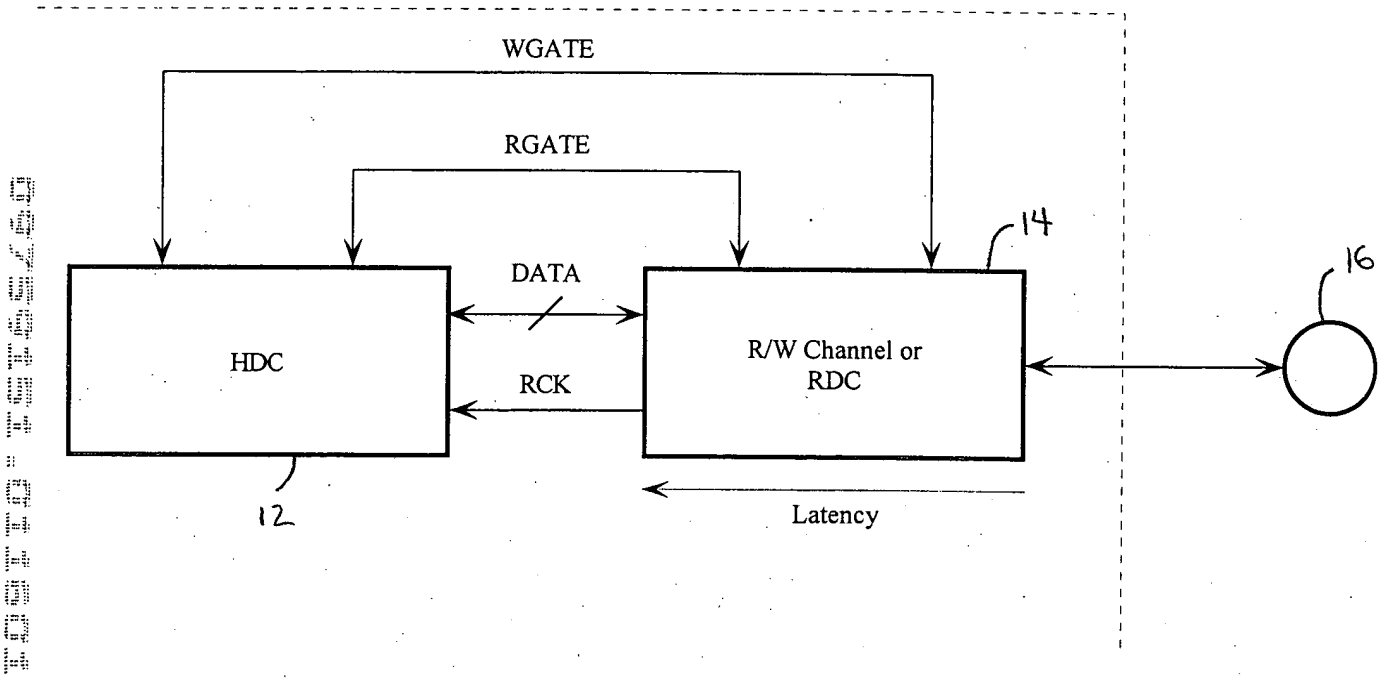

Fig. 1

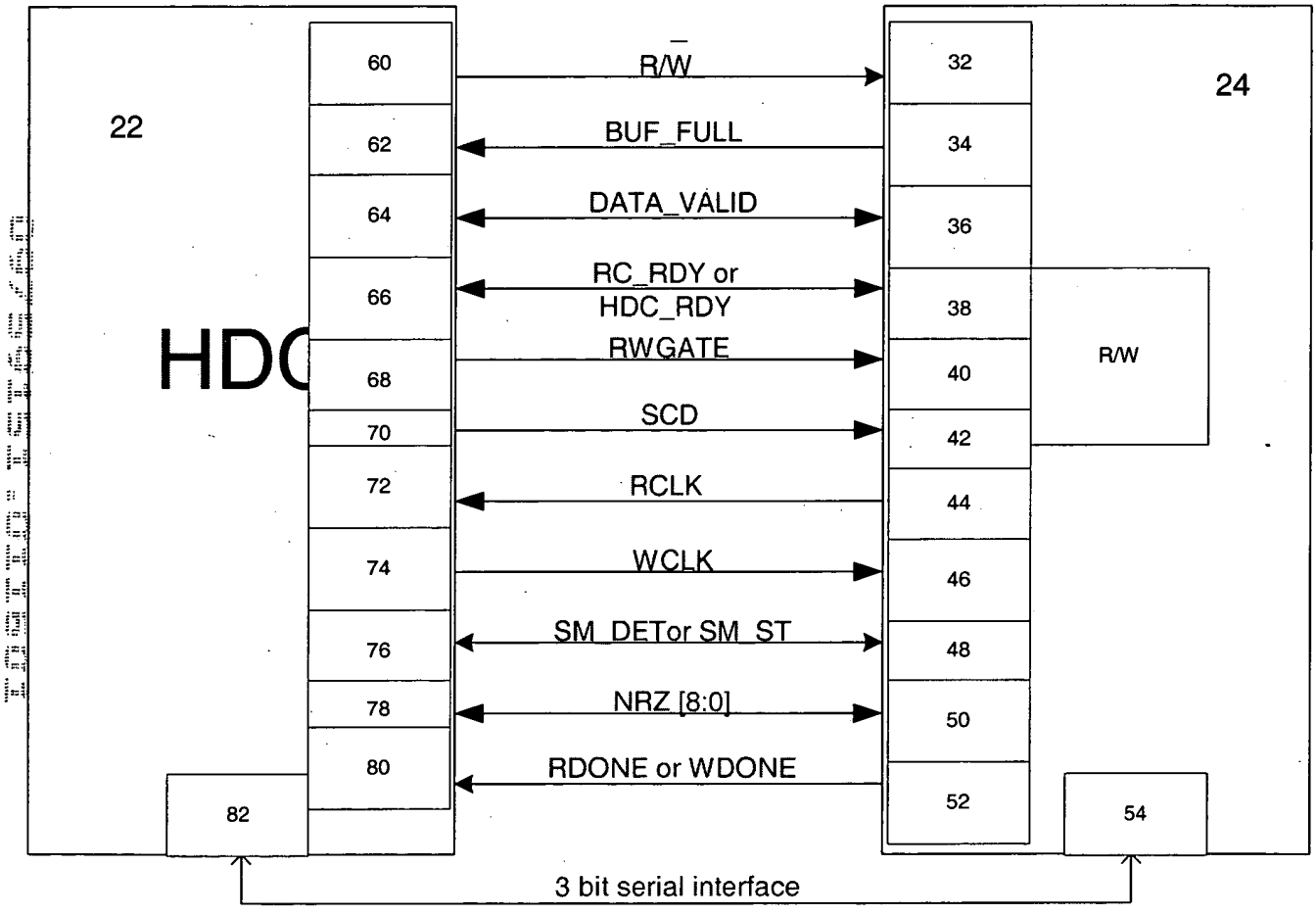
20
22
HDC
24
60
62
64
66
68
70
72
74
76
78
80
82
32
34
36
38
40
42
44
46
48
50
52
54
R/W
R/W
BUF_FULL
DATA_VALID
RC_RDY or
HDC_RDY
RWGATE
SCD
RCLK
WCLK
SM_DETor SM_ST
NRZ [8:0]
RDONE or WDONE
3 bit serial interface

Fig. 2

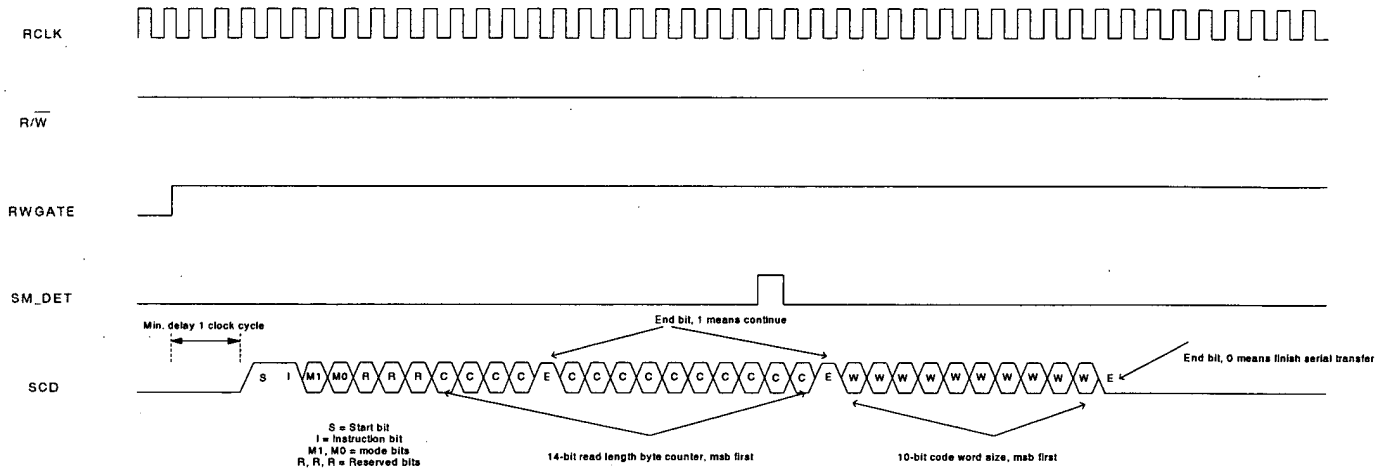
RCLK
R/W
RWGATE
SM_DET
SCD
Min. delay 1 clock cycle
End bit, 1 means continue
End bit, 0 means finish serial transfer
S = Start bit
I = Instruction bit
M1, M0 = mode bits
R, R, R = Reserved bits
14-bit read length byte counter, msb first
10-bit code word size, msb first

Fig. 3

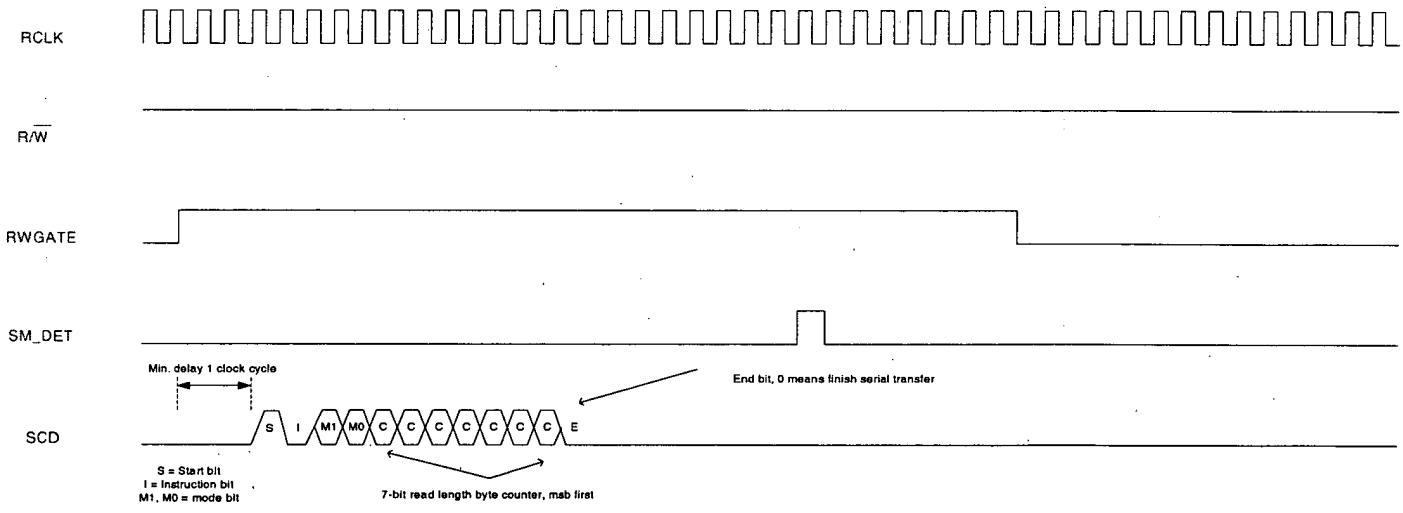
RCLK
R/W
RWGATE
SM_DET
SCD
Min. delay 1 clock cycle
End bit, 0 means finish serial transfer
S = Start bit
I = Instruction bit
M1, M0 = mode bit
7-bit read length byte counter, msb first

Fig. 4

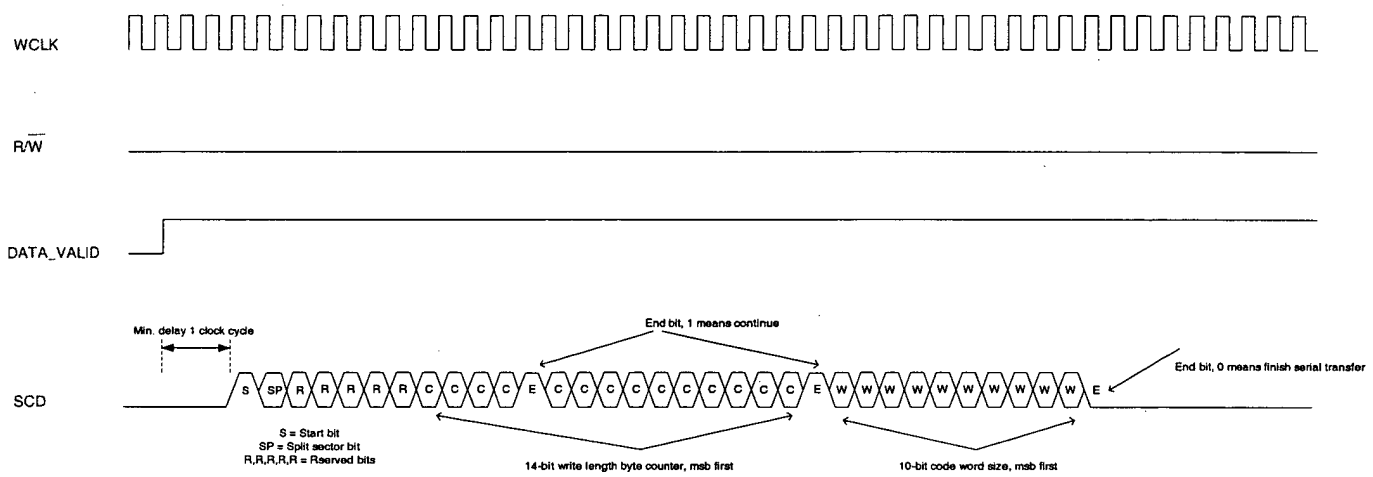
WCLK
R/W
DATA_VALID
SCD
Min. delay 1 clock cycle
End bit, 1 means continue
End bit, 0 means finish serial transfer
S SP R R R R R C C C C E C C C C C C C C C C E W W W W W W W W W E
S = Start bit
SP = Split sector bit
R,R,R,R,R = Reserved bits
14-bit write length byte counter, msb first
10-bit code word size, msb first

Fig. 5

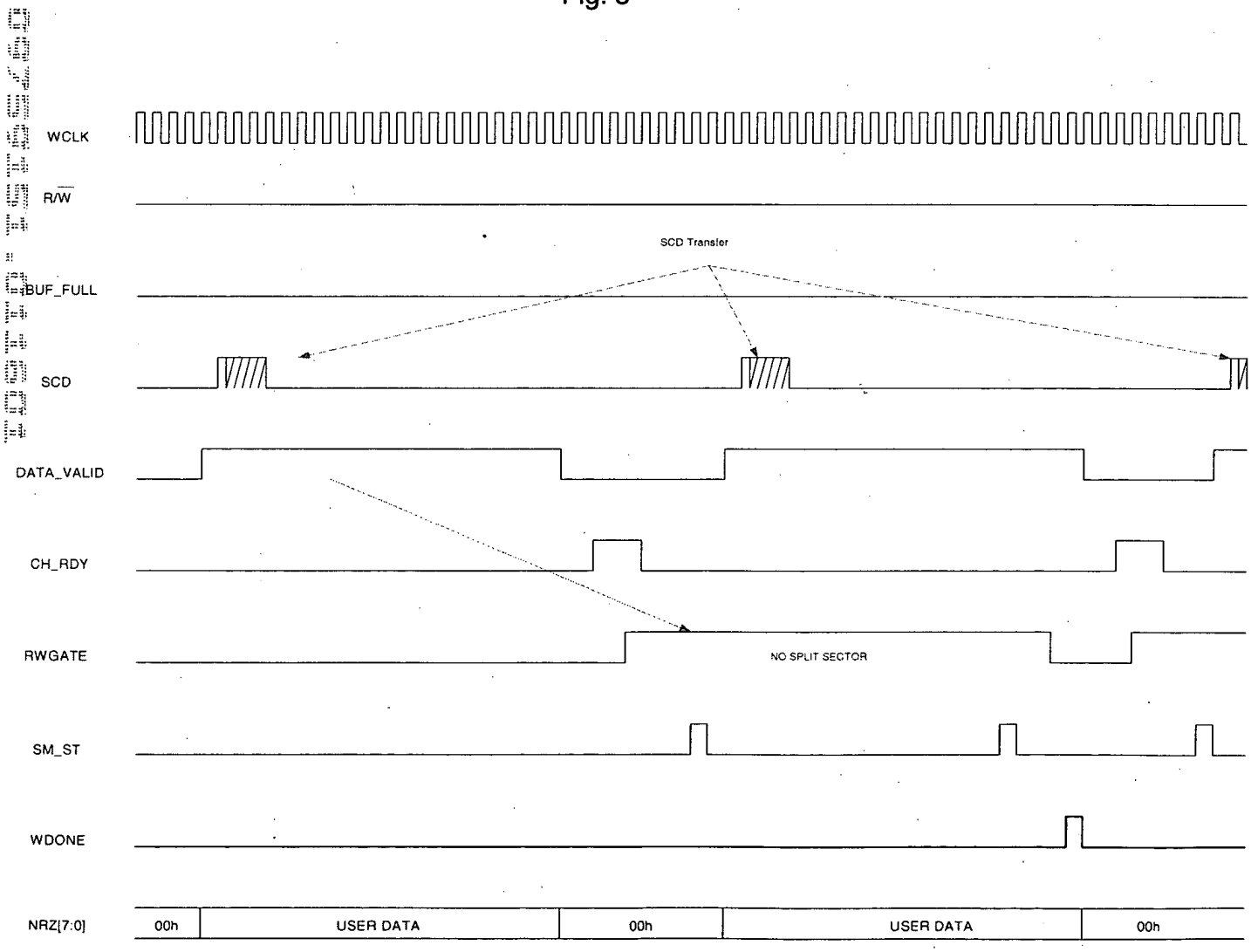
WCLK
R/W
SCD Transfer
BUF_FULL
SCD
DATA_VALID
CH_RDY
RWGATE
NO SPLIT SECTOR
SM_ST
WDONE
NRZ[7:0]
00h
USER DATA
00h
USER DATA
00h

Fig. 6

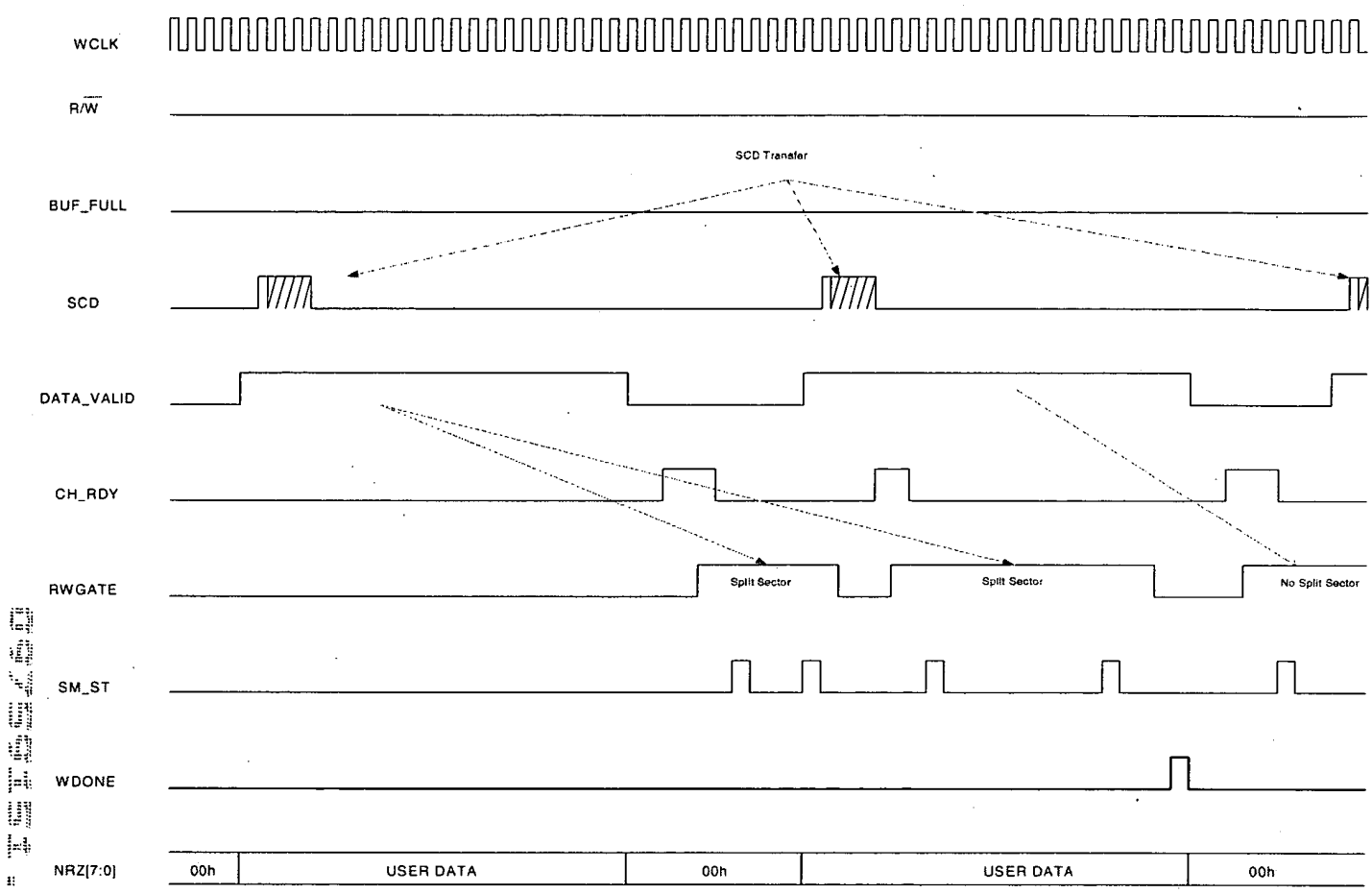
WCLK
R/W
SCD Transfer
BUF_FULL
SCD
DATA_VALID
CH_RDY
RWGATE
Split Sector
Split Sector
No Split Sector
SM_ST
WDONE
NRZ[7:0]
00h
USER DATA
00h
USER DATA
00h

Fig. 7

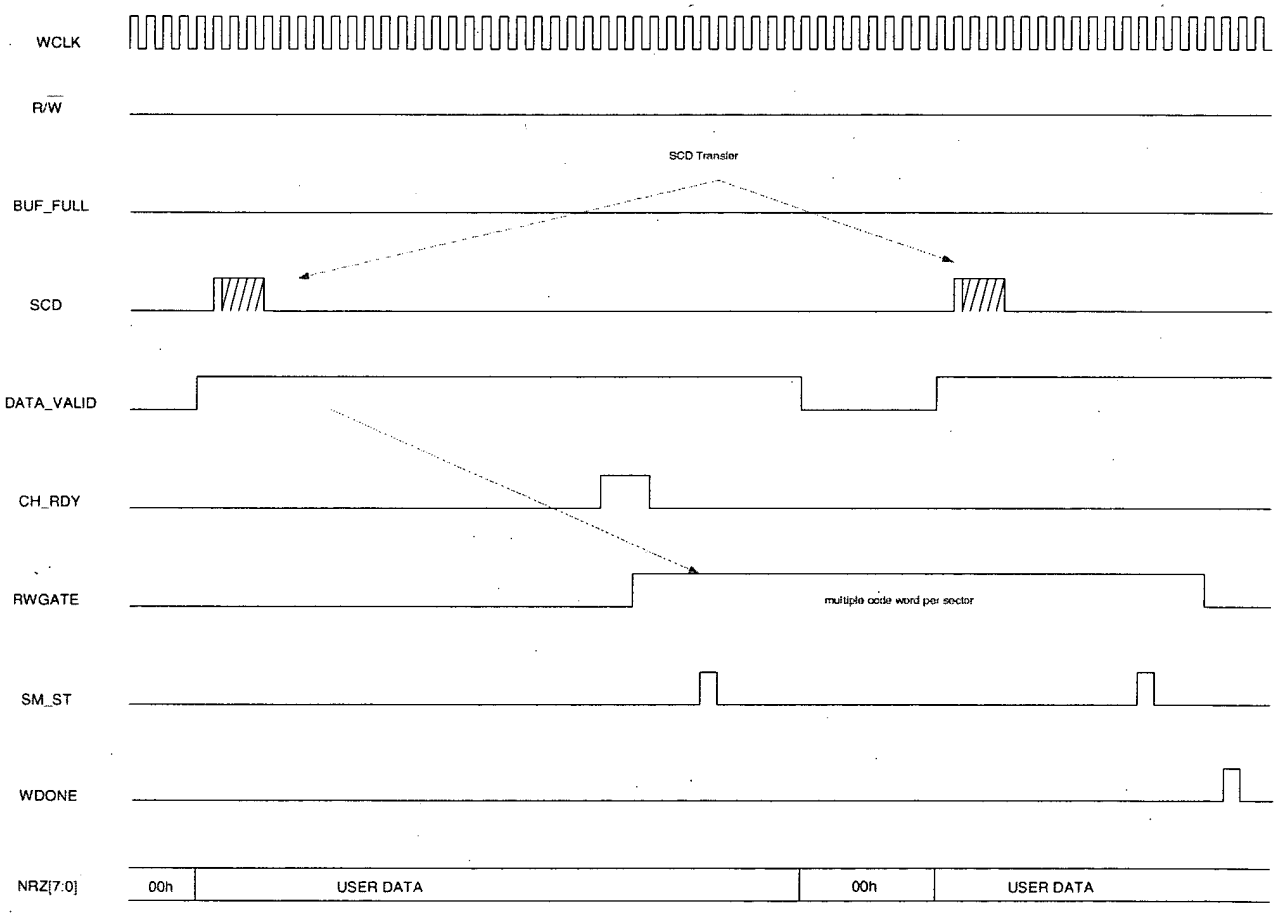
WCLK
R/W
SCD Transfer
BUF_FULL
SCD
DATA_VALID
CH_RDY
RWGATE
multiple code word per sector
SM_ST
WDONE
NRZ[7:0]
00h
USER DATA
00h
USER DATA

Fig. 8

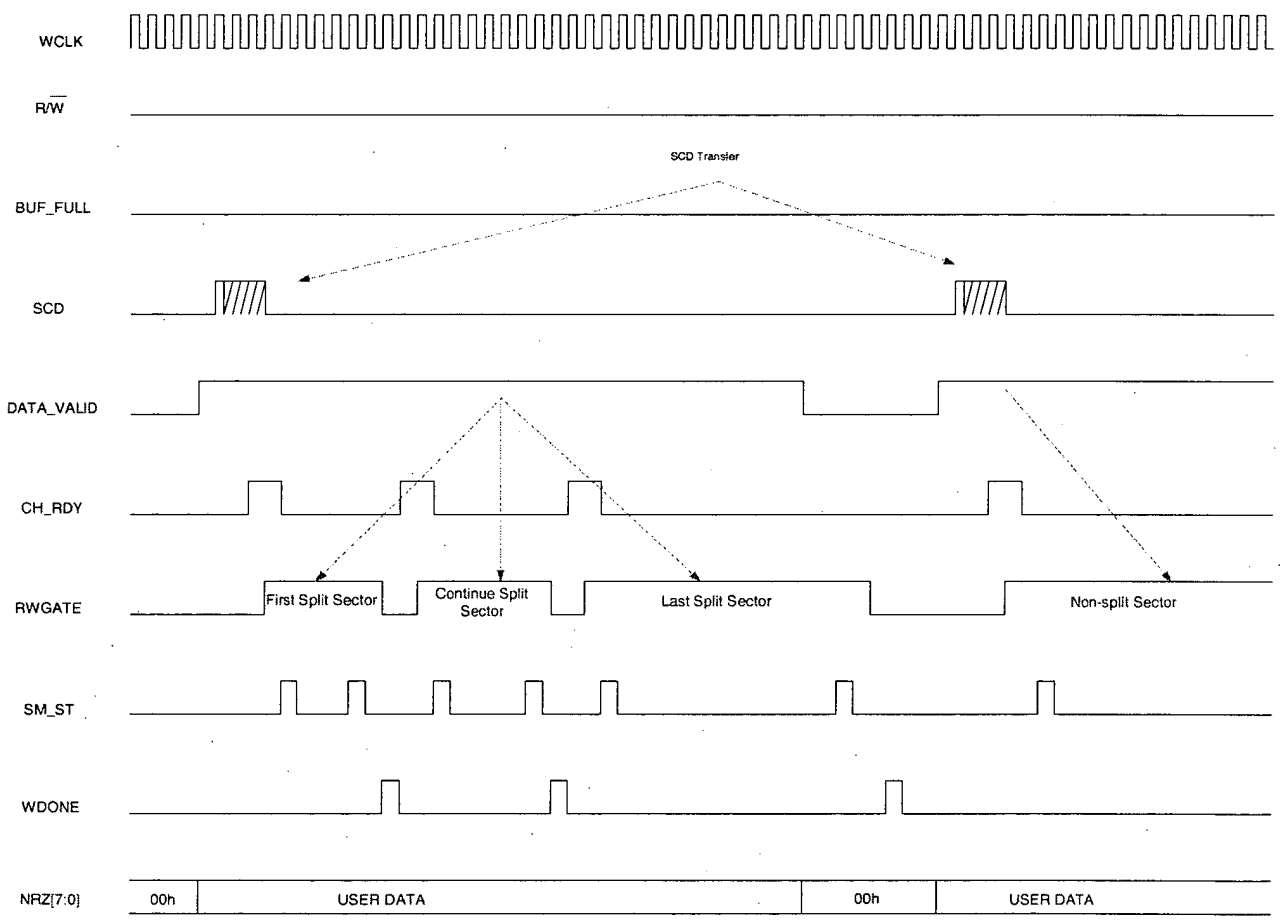
WCLK
R/W
SCD Transfer
BUF_FULL
SCD
DATA_VALID
CH_RDY
RWGATE
First Split Sector
Continue Split Sector
Last Split Sector
Non-split Sector
SM_ST
WDONE
NRZ[7:0]
00h
USER DATA
00h
USER DATA

Fig. 9

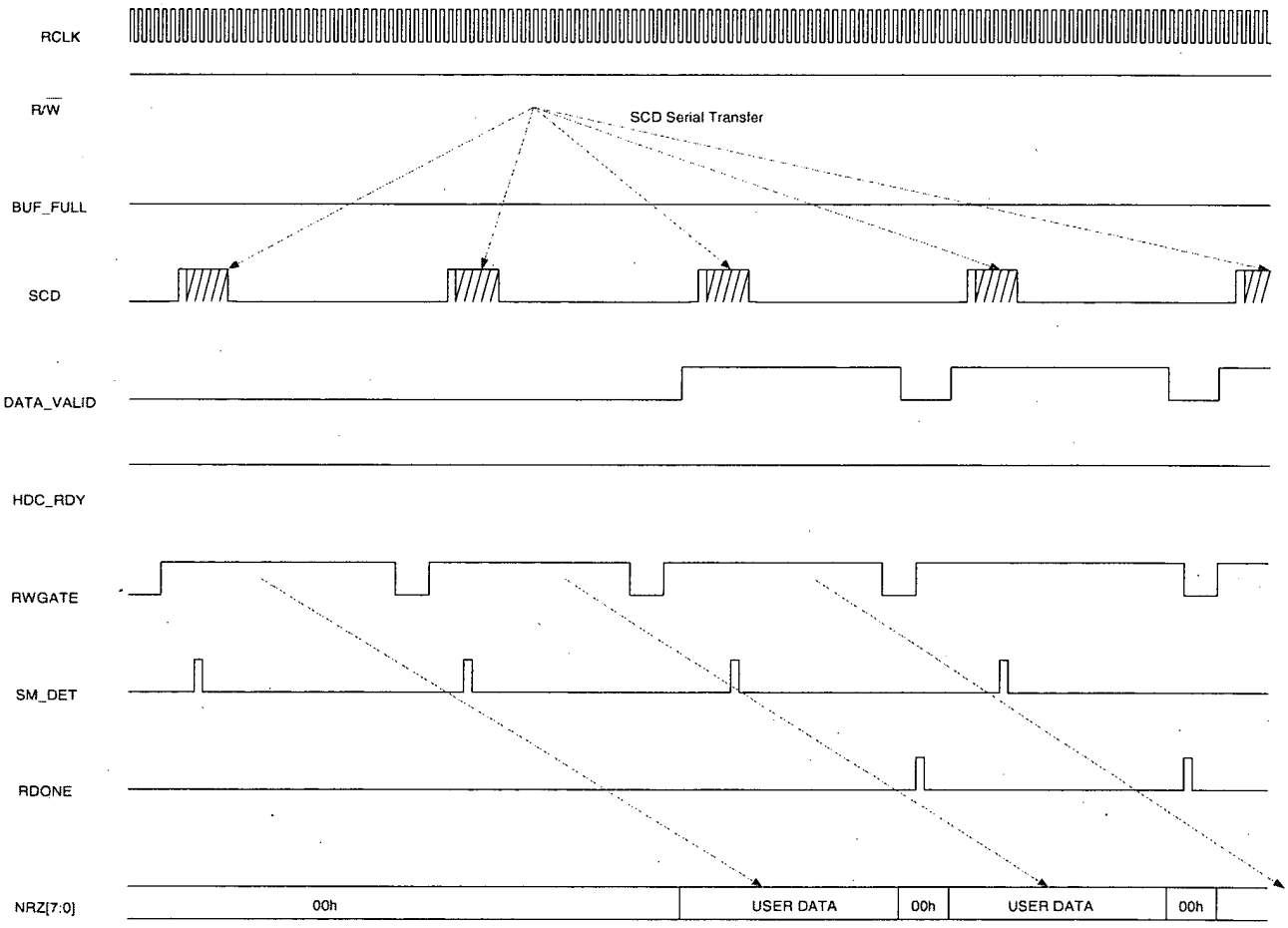
RCLK
R/W
SCD Serial Transfer
BUF_FULL
SCD
DATA_VALID
HDC_RDY
RWGATE
SM_DET
RDONE
NRZ[7:0]
00h
USER DATA
00h
USER DATA
00h

Fig. 10

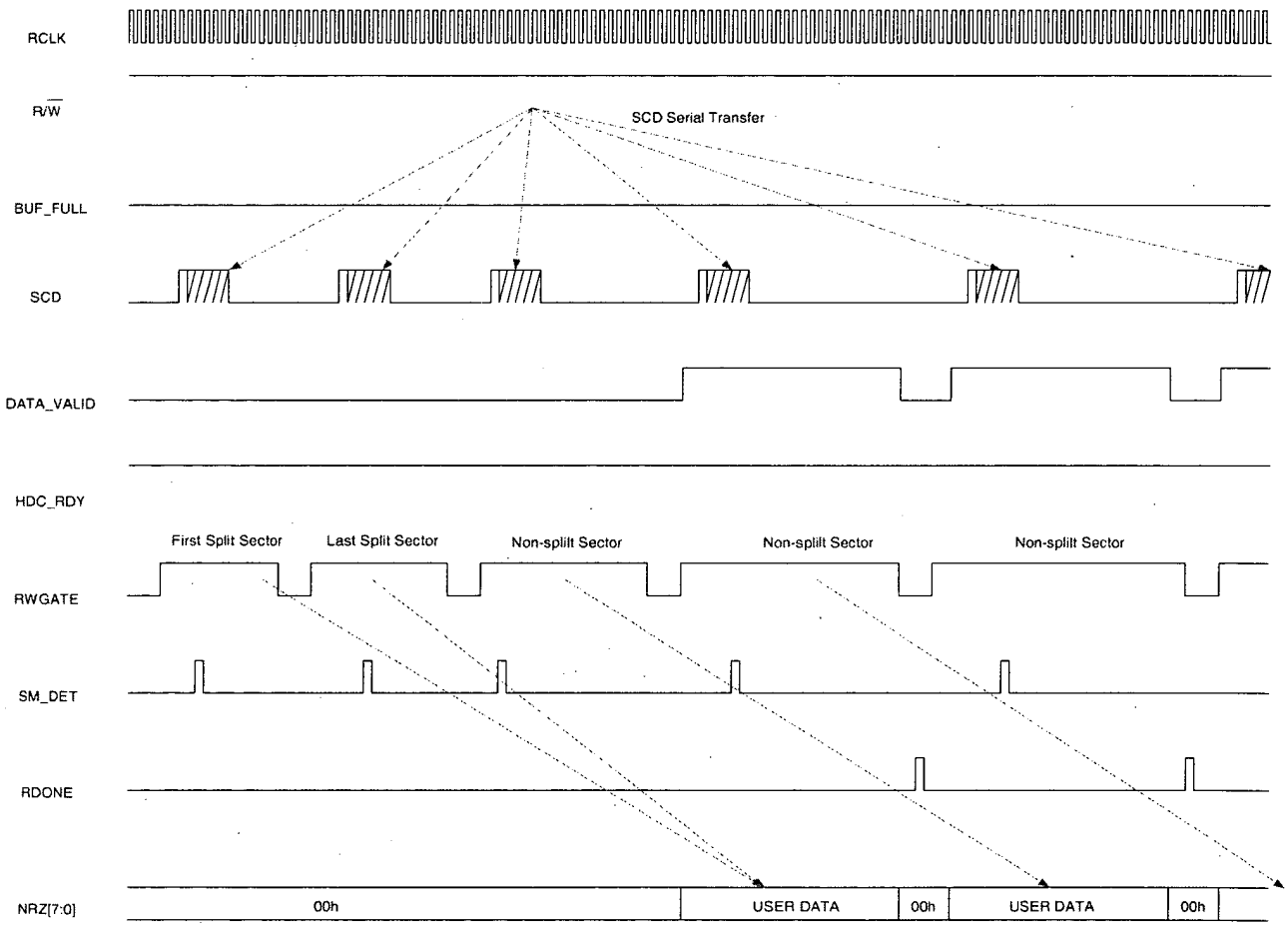
RCLK
R/W
SCD Serial Transfer
BUF_FULL
SCD
DATA_VALID
HDC_RDY
First Split Sector
Last Split Sector
Non-split Sector
Non-split Sector
Non-split Sector
RWGATE
SM_DET
RDONE
NRZ[7:0]
00h
USER DATA
00h
USER DATA
00h

Fig. 11

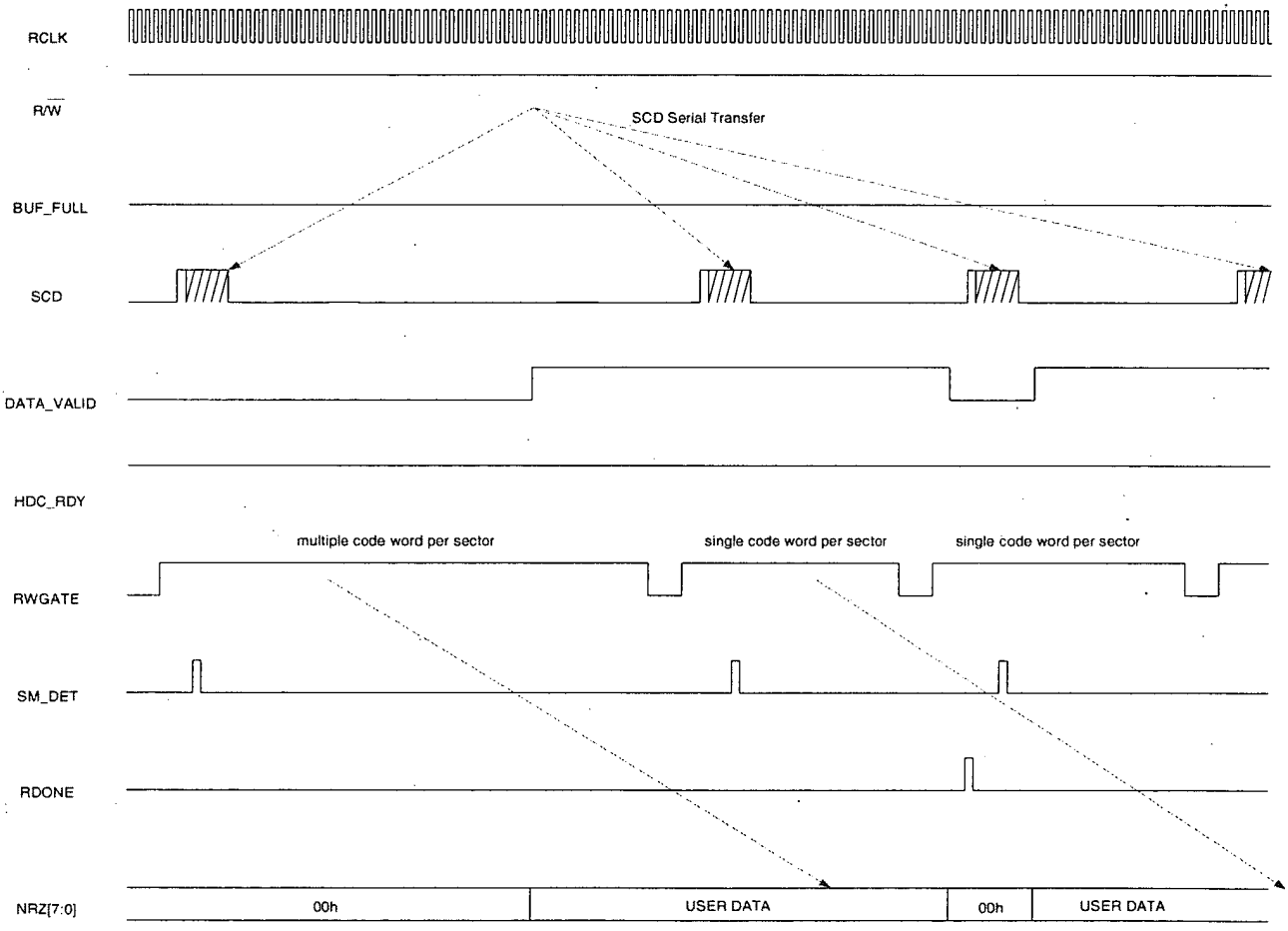
RCLK
R/W
SCD Serial Transfer
BUF_FULL
SCD
DATA_VALID
HDC_RDY
multiple code word per sector
single code word per sector
single code word per sector
RWGATE
SM_DET
RDONE
NRZ[7:0]
00h
USER DATA
00h
USER DATA

Fig. 12

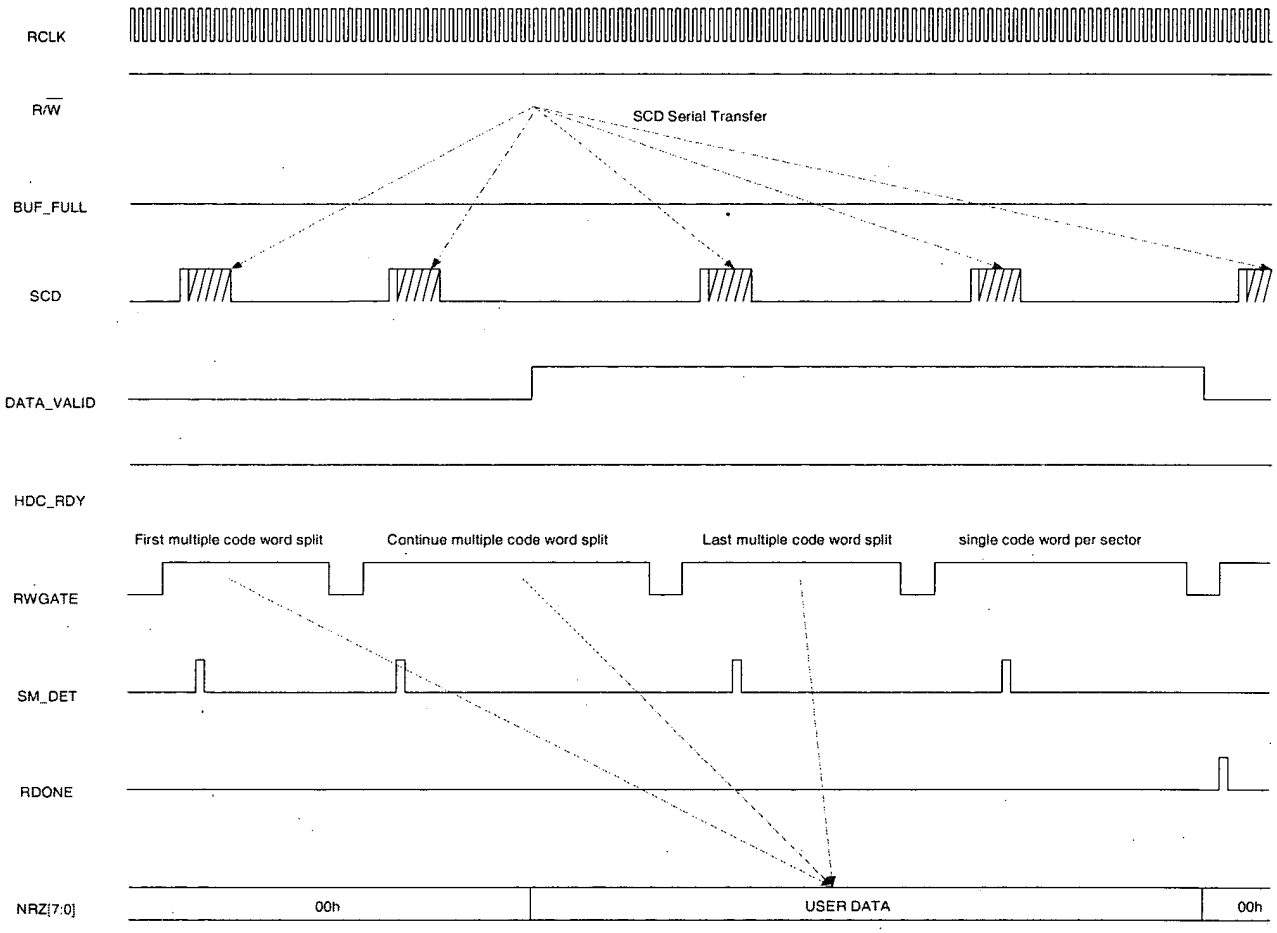
RCLK
R/W
SCD Serial Transfer
BUF_FULL
SCD
DATA_VALID
HDC_RDY
First multiple code word split
Continue multiple code word split
Last multiple code word split
single code word per sector
RWGATE
SM_DET
RDONE
NRZ[7:0]
00h
USER DATA
00h

Fig. 13

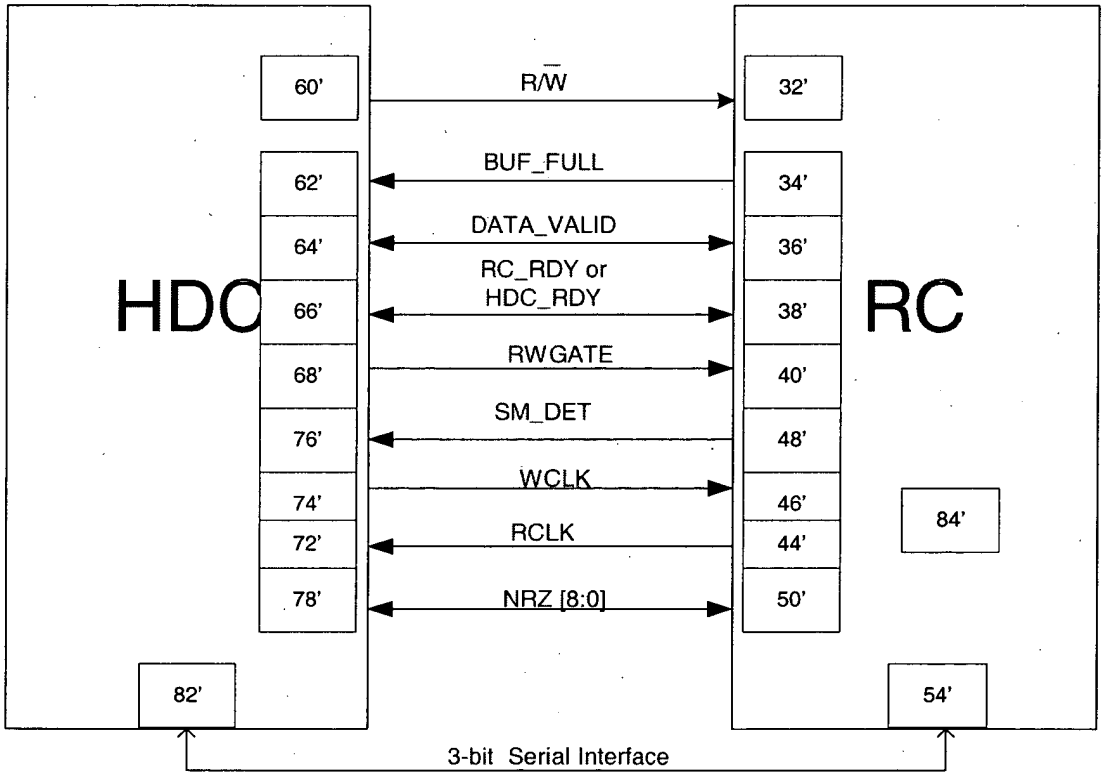
20'
22'
24'
HDC
RC
60'
62'
64'
66'
68'
76'
74'
72'
78'
32'
34'
36'
38'
40'
48'
46'
44'
50'
84'
82'
54'
R/W
BUF_FULL
DATA_VALID
RC_RDY or
HDC_RDY
RWGATE
SM_DET
WCLK
RCLK
NRZ [8:0]
3-bit Serial Interface

Fig. 14

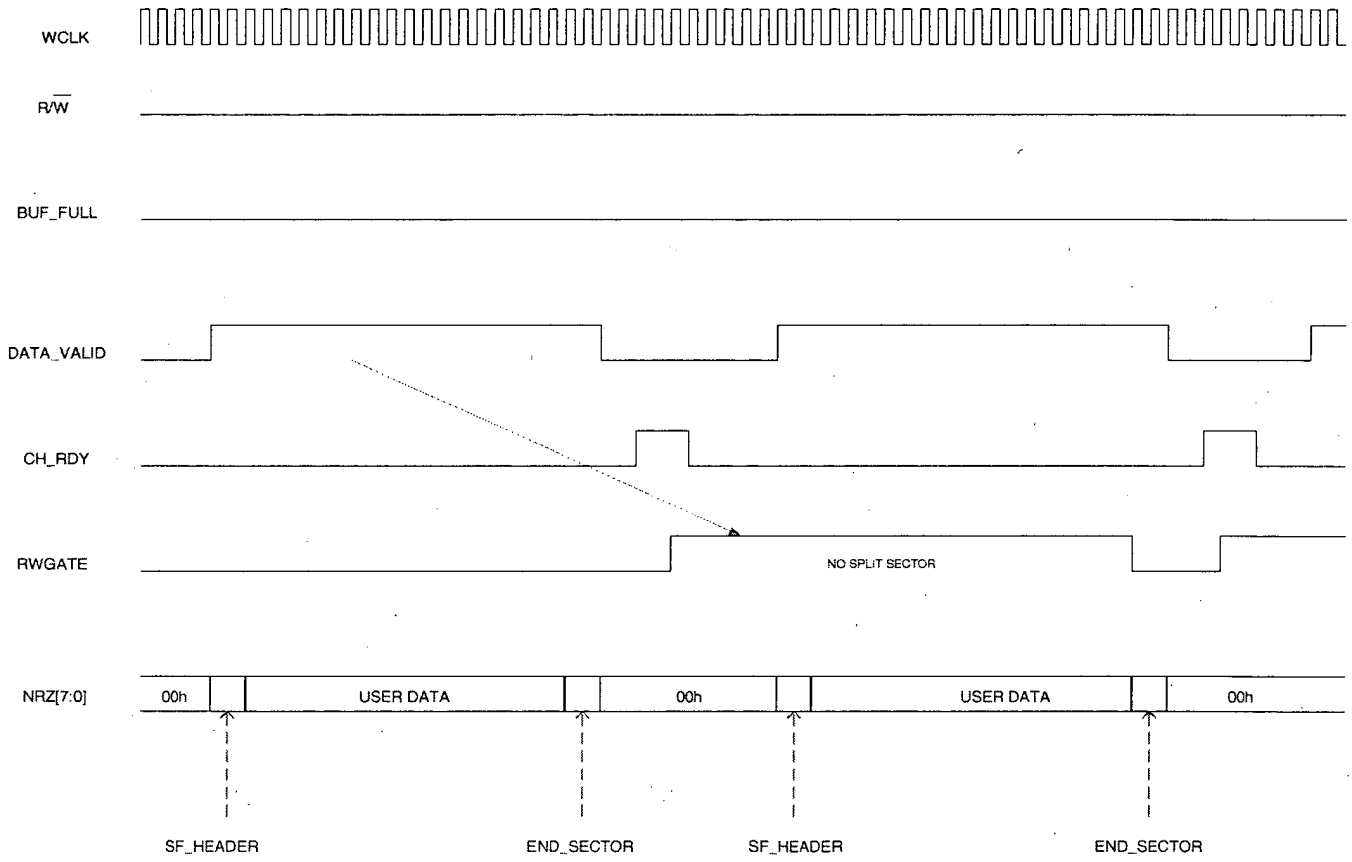
WCLK
R/W
BUF_FULL
DATA_VALID
CH_RDY
RWGATE
NO SPLIT SECTOR
NRZ[7:0]
00h
USER DATA
00h
USER DATA
00h
SF_HEADER
END_SECTOR
SF_HEADER
END_SECTOR

Fig. 15

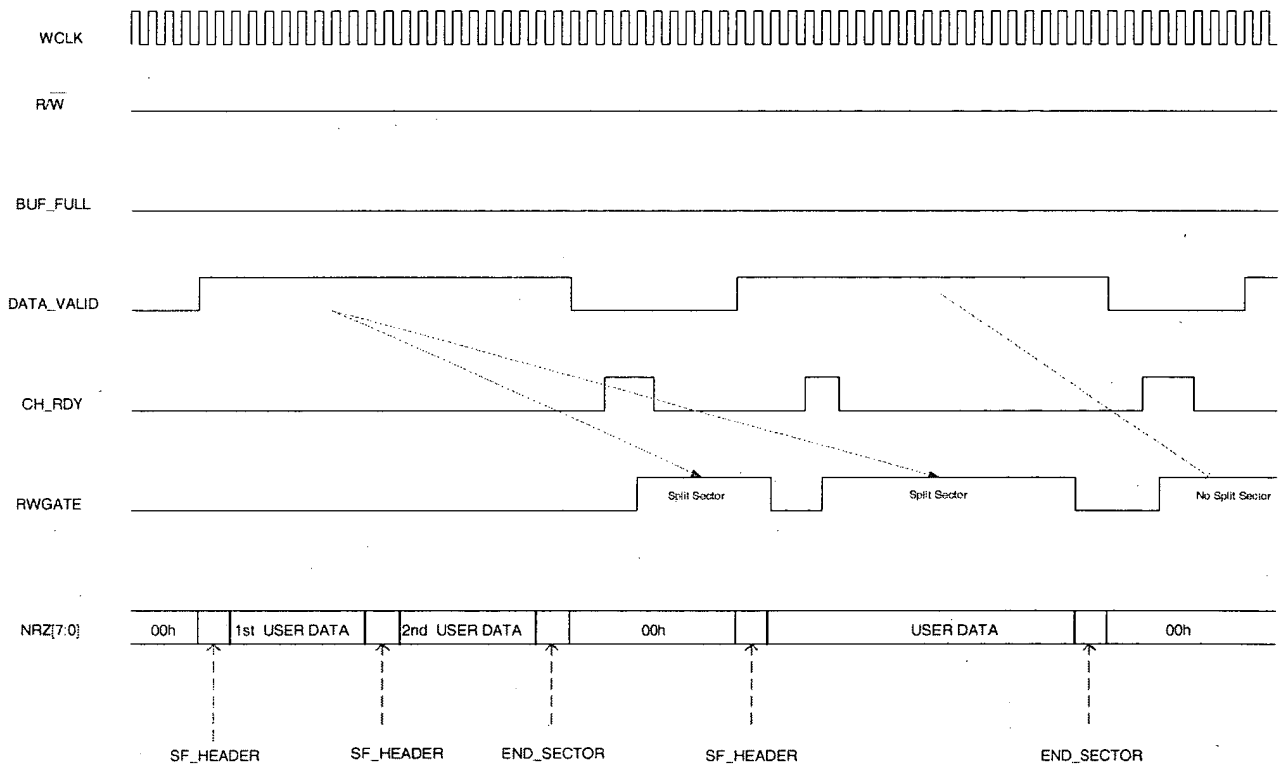
WCLK
R/W
BUF_FULL
DATA_VALID
CH_RDY
RWGATE
Split Sector
Split Sector
No Split Sector
NRZ[7:0]
00h
1st USER DATA
2nd USER DATA
00h
USER DATA
00h
SF_HEADER
SF_HEADER
END_SECTOR
SF_HEADER
END_SECTOR

Fig. 16

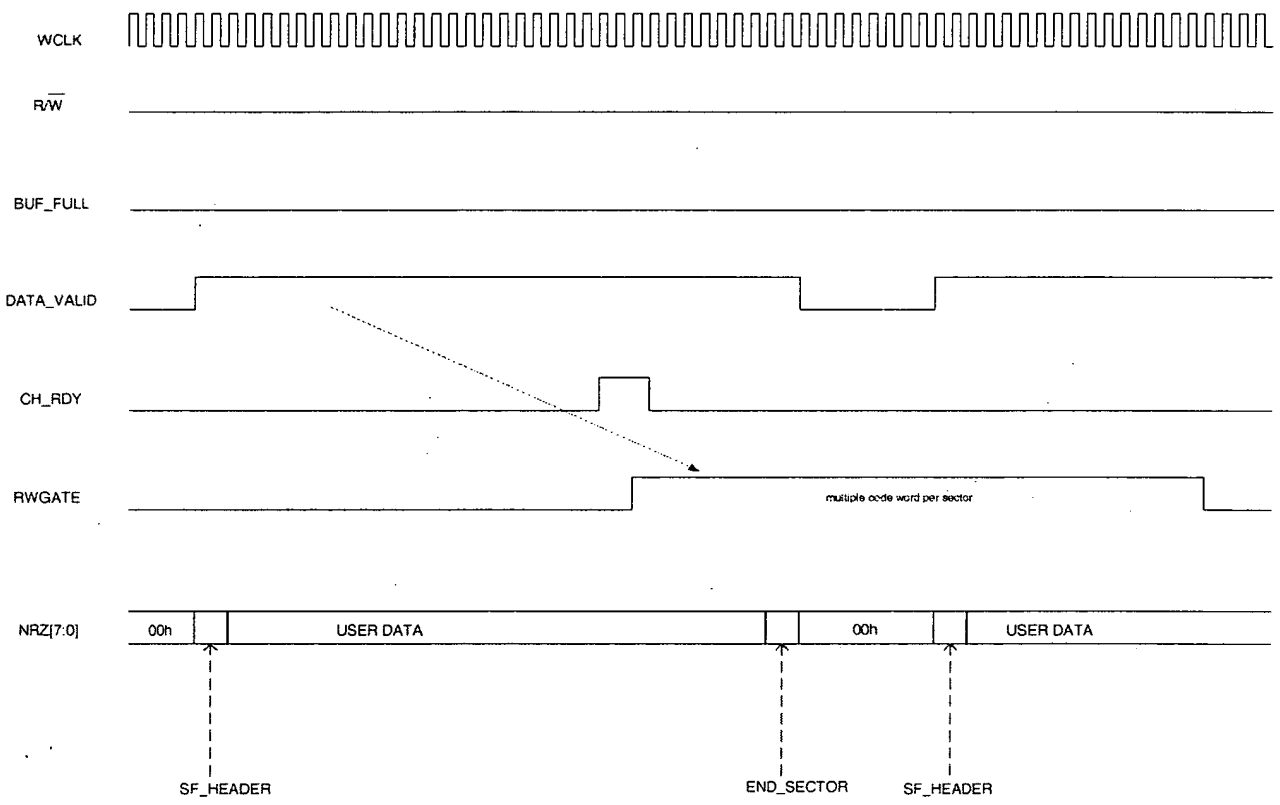
WCLK
R/W
BUF_FULL
DATA_VALID
CH_RDY
RWGATE
multiple code word per sector
NRZ[7:0]
00h
USER DATA
00h
USER DATA
SF_HEADER
END_SECTOR
SF_HEADER

Fig. 17

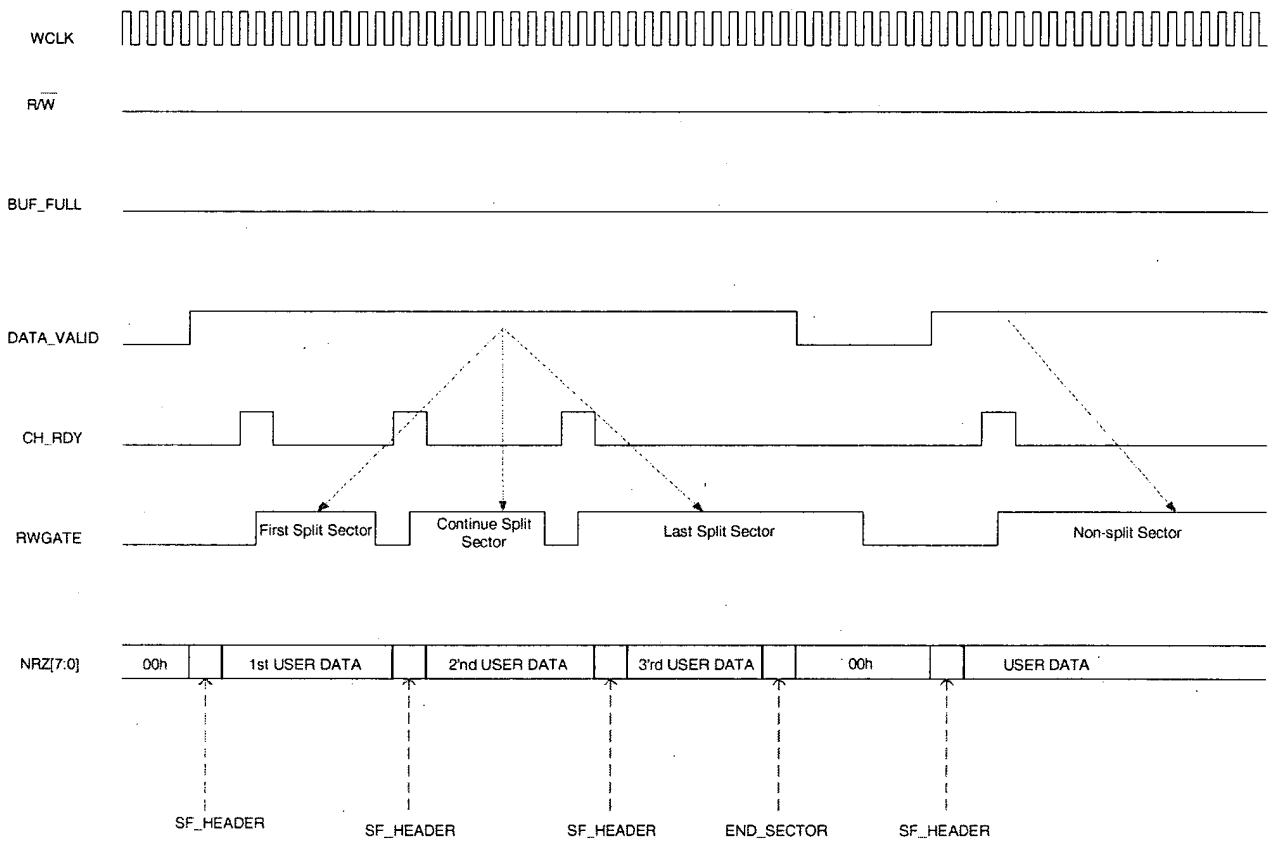
WCLK
R/W
BUF_FULL
DATA_VALID
CH_RDY
RWGATE
First Split Sector
Continue Split Sector
Last Split Sector
Non-split Sector
NRZ[7:0]
00h
1st USER DATA
2'nd USER DATA
3'rd USER DATA
00h
USER DATA
SF_HEADER
SF_HEADER
SF_HEADER
END_SECTOR
SF_HEADER

Fig. 18

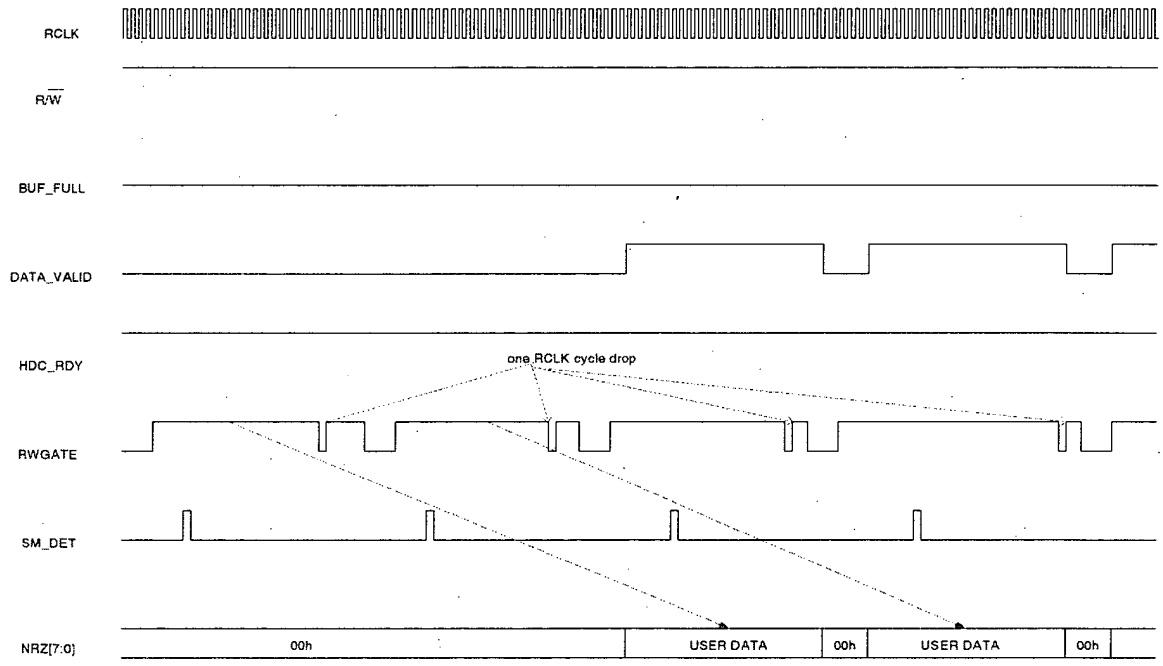
RCLK
R/W
BUF_FULL
DATA_VALID
HDC_RDY
one RCLK cycle drop
RWGATE
SM_DET
NRZ[7:0]
00h
USER DATA
00h
USER DATA
00h

Fig. 19

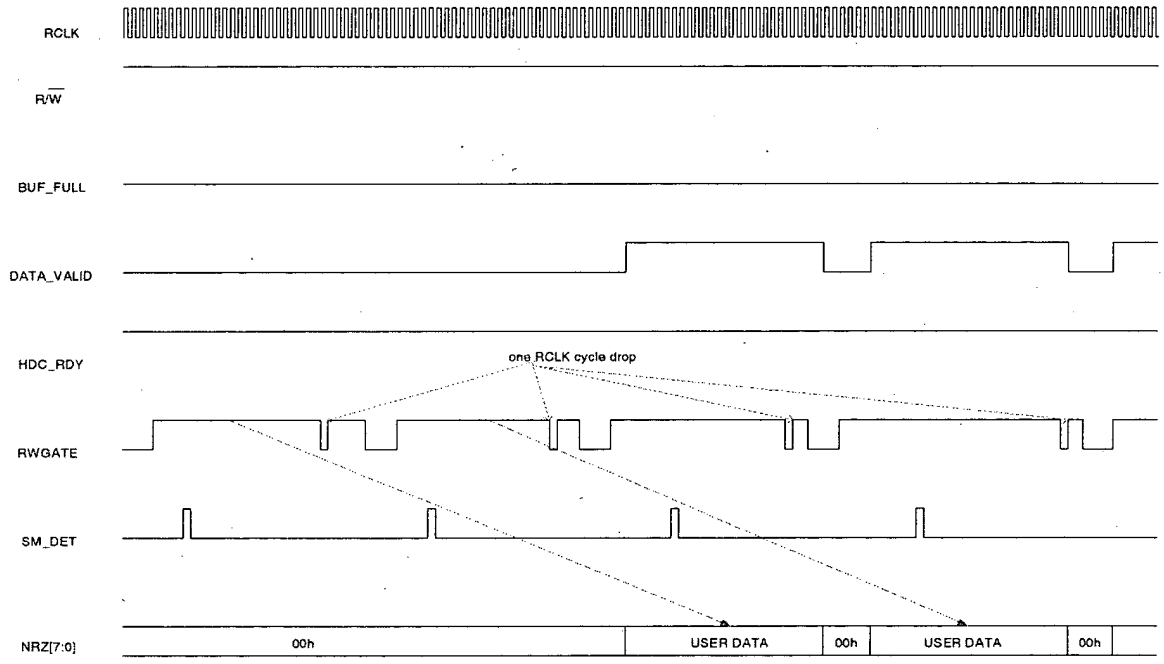
RCLK
R/W
BUF_FULL
DATA_VALID
HDC_RDY
one RCLK cycle drop
RWGATE
SM_DET
NRZ[7:0]
00h
USER DATA
00h
USER DATA
00h

Fig. 20

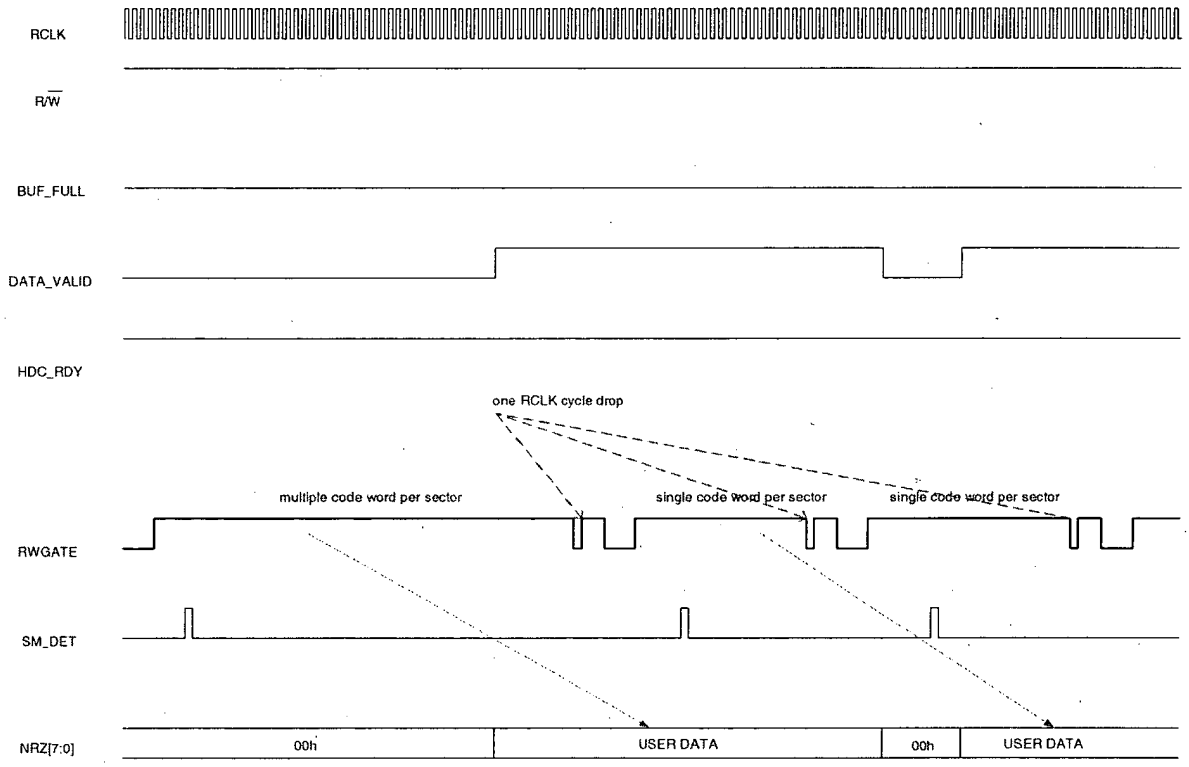
RCLK
R/W
BUF_FULL
DATA_VALID
HDC_RDY
one RCLK cycle drop
multiple code word per sector
single code word per sector
single code word per sector
RWGATE
SM_DET
NRZ[7:0]
00h
USER DATA
00h
USER DATA

Fig. 21

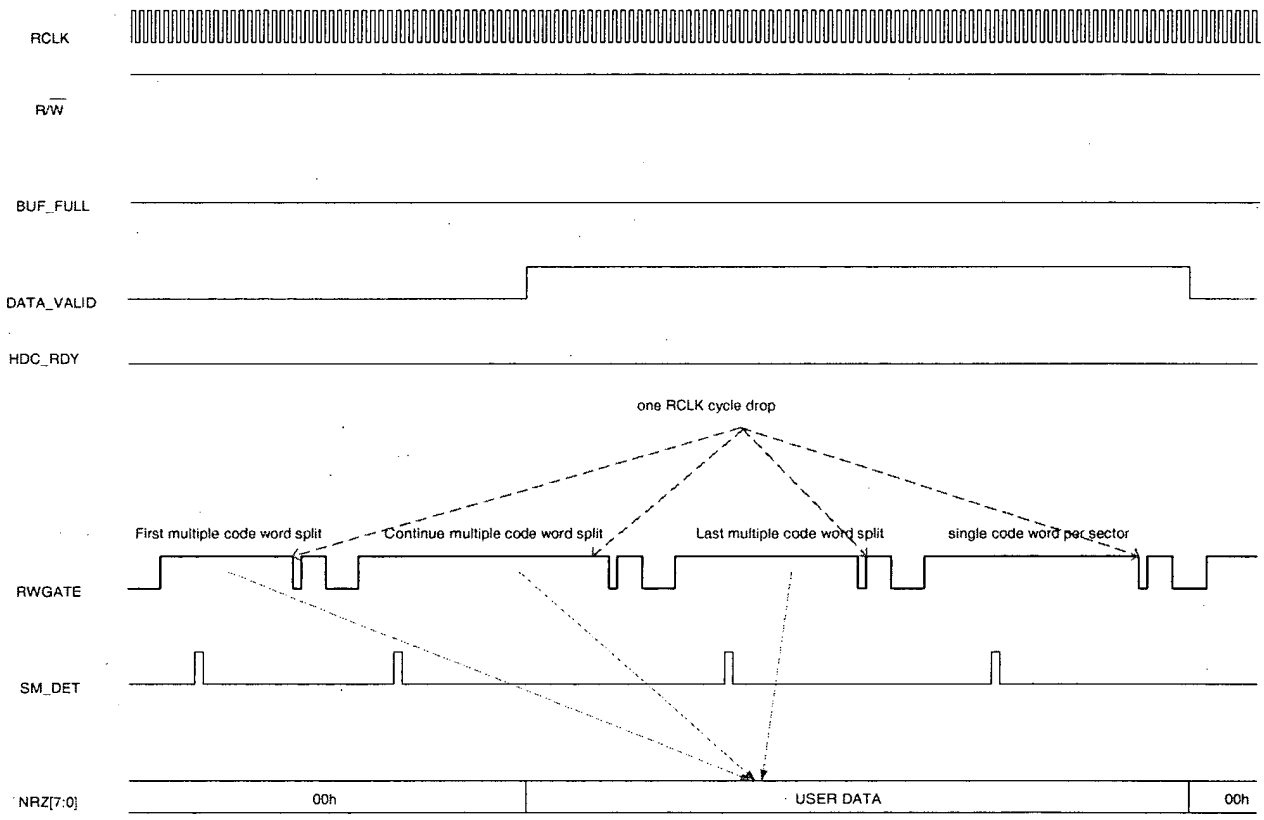
RCLK
R/W
BUF_FULL
DATA_VALID
HDC_RDY
one RCLK cycle drop
First multiple code word split
Continue multiple code word split
Last multiple code word split
single code word per sector
RWGATE
SM_DET
NRZ[7:0]
00h
USER DATA
00h

Fig. 22

SF_HEADER	User data for Multiple codewords	END_SECTOR

Fig. 23

SF_HEADER	1st set user data	SF_HEADER	2nd set user data	SF_HEADER	3rd set user data	END_SECTOR

Fig. 24

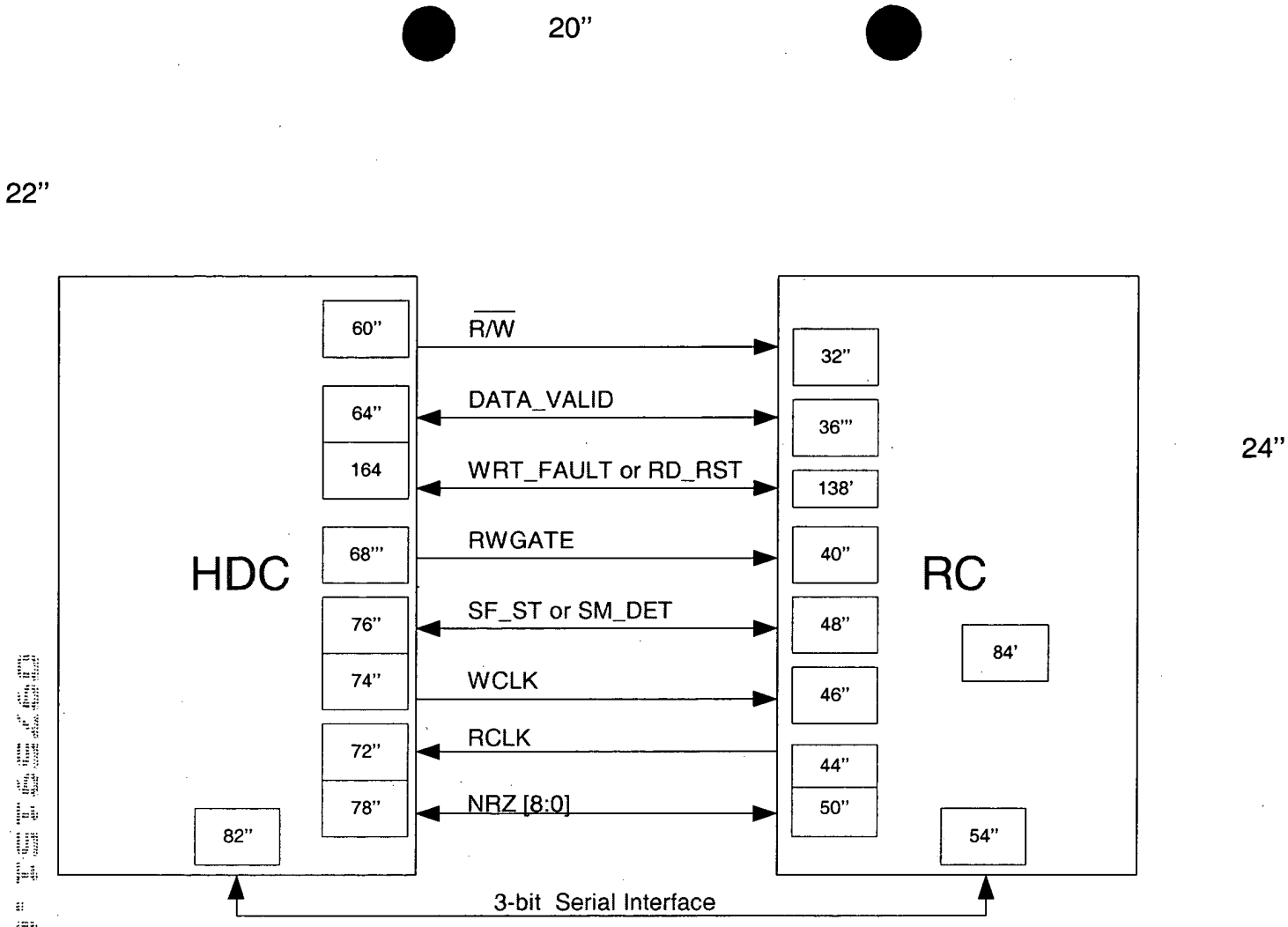
20"
22"
24"
HDC
RC
60"
64"
164
68"'
76"
74"
72"
78"
82"
R/W
DATA_VALID
WRT_FAULT or RD_RST
RWGATE
SF_ST or SM_DET
WCLK
RCLK
NRZ [8:0]
32"
36"'
138'
40"
48"
46"
44"
50"
84'
54"
3-bit Serial Interface

Fig. 25

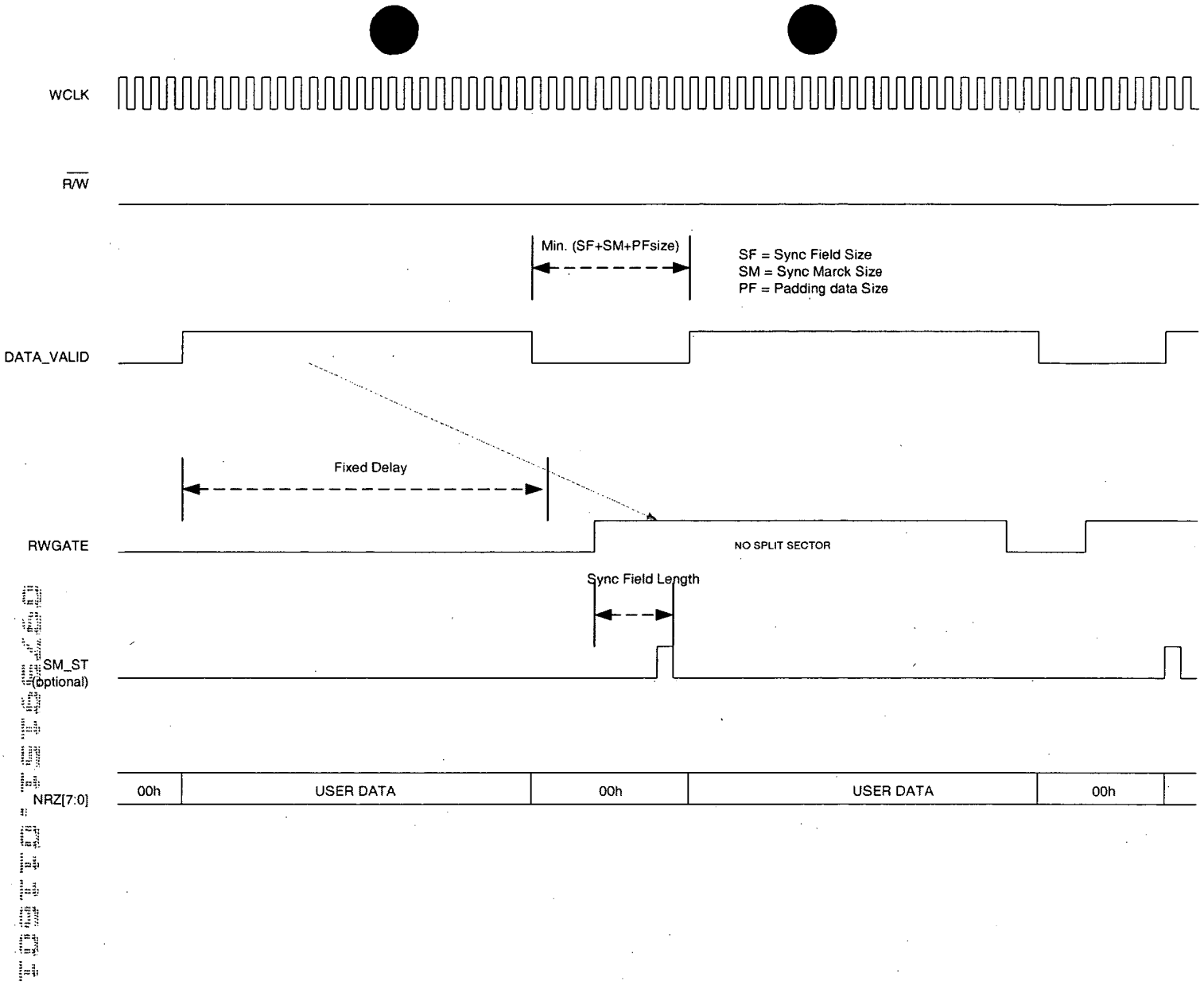
WCLK
R/W
Min. (SF+SM+PFsize)
SF = Sync Field Size
SM = Sync Marck Size
PF = Padding data Size
DATA_VALID
Fixed Delay
RWGATE
NO SPLIT SECTOR
Sync Field Length
SM_ST
(optional)
NRZ[7:0]
00h
USER DATA
00h
USER DATA
00h

Fig. 26

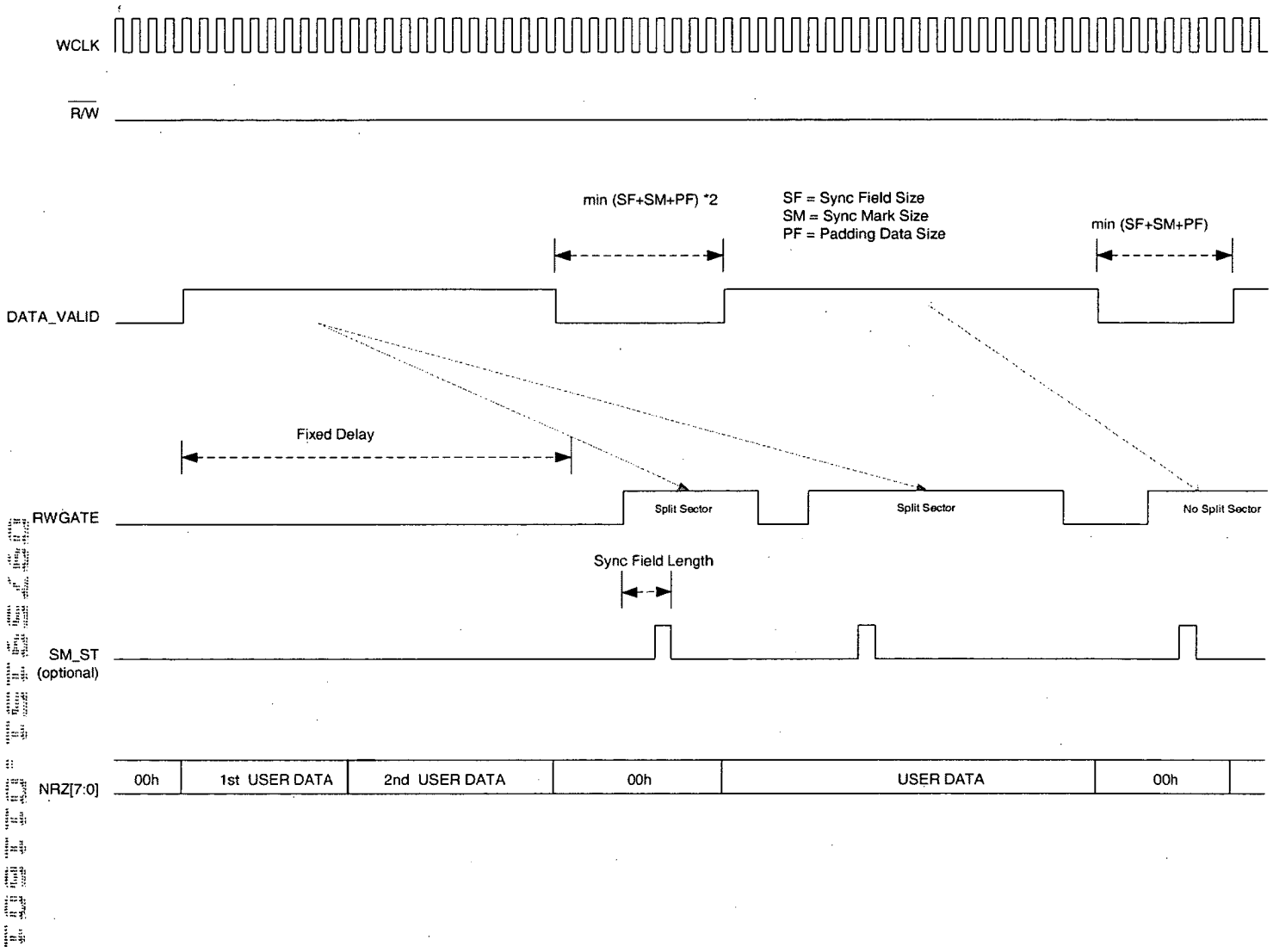
WCLK
R/W
min (SF+SM+PF) *2
SF = Sync Field Size
SM = Sync Mark Size
PF = Padding Data Size
min (SF+SM+PF)
DATA_VALID
Fixed Delay
RWGATE
Split Sector
Split Sector
No Split Sector
Sync Field Length
SM_ST
(optional)
NRZ[7:0]
00h
1st USER DATA
2nd USER DATA
00h
USER DATA
00h

Fig. 27

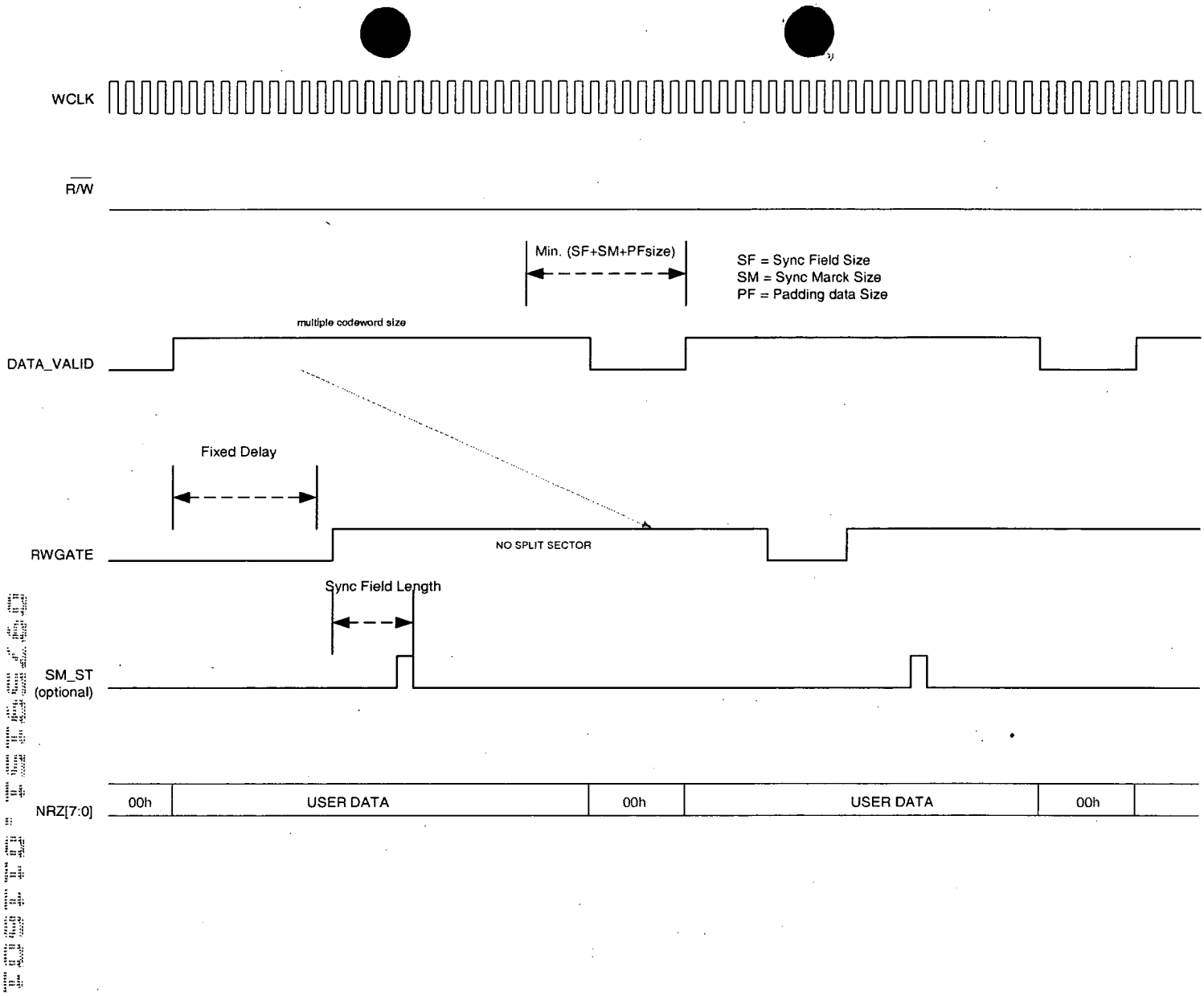
WCLK
R/W
Min. (SF+SM+PFsize)
SF = Sync Field Size
SM = Sync Marck Size
PF = Padding data Size
multiple codeword size
DATA_VALID
Fixed Delay
RWGATE
NO SPLIT SECTOR
Sync Field Length
SM_ST
(optional)
NRZ[7:0]
00h
USER DATA
00h
USER DATA
00h

Fig. 28

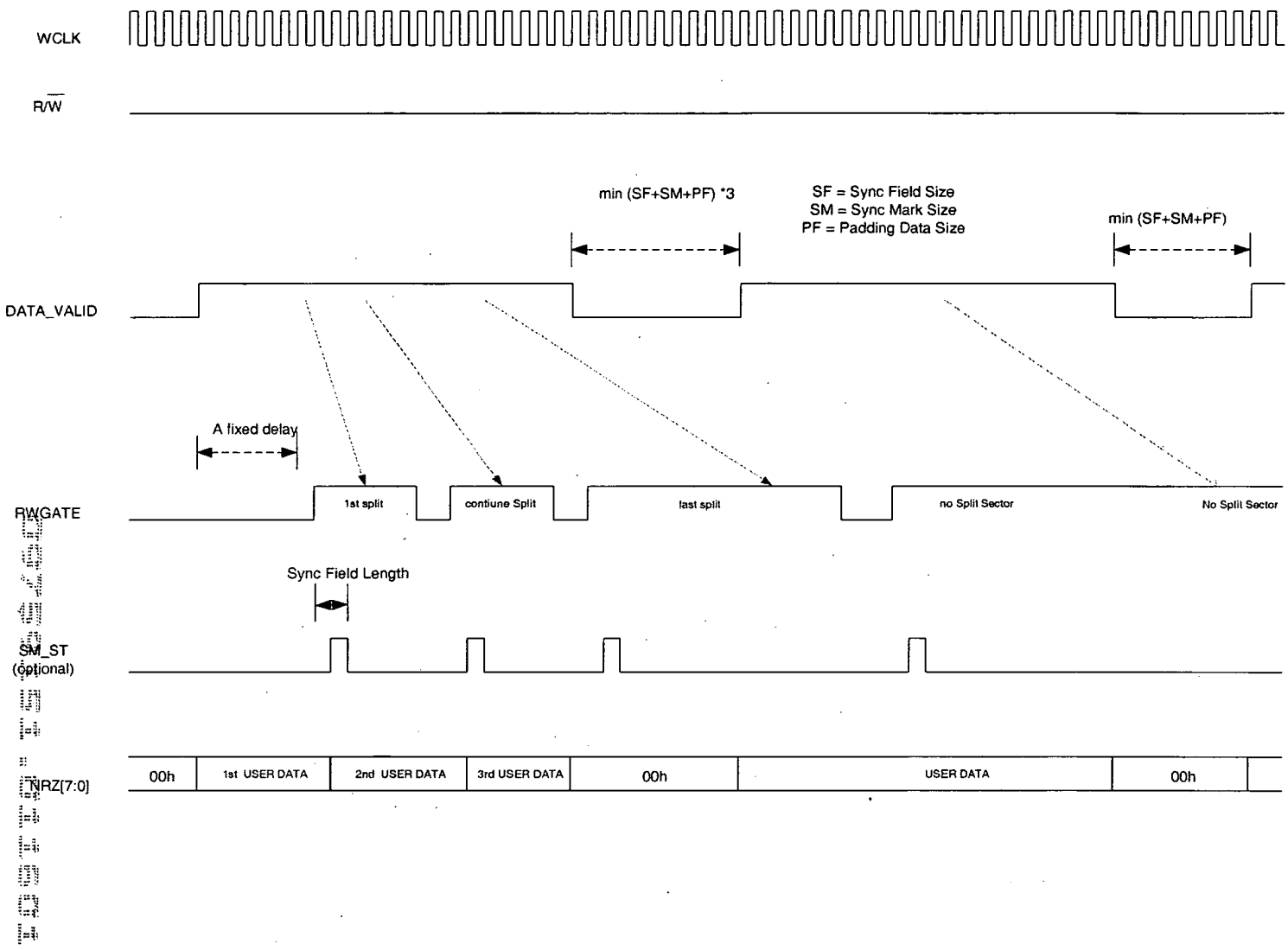
WCLK
R/W
min (SF+SM+PF) *3
SF = Sync Field Size
SM = Sync Mark Size
PF = Padding Data Size
min (SF+SM+PF)
DATA_VALID
A fixed delay
RWGATE
1st split
contiune Split
last split
no Split Sector
No Split Sector
Sync Field Length
SM_ST
(optional)
NRZ[7:0]
00h
1st USER DATA
2nd USER DATA
3rd USER DATA
00h
USER DATA
00h

Fig. 29

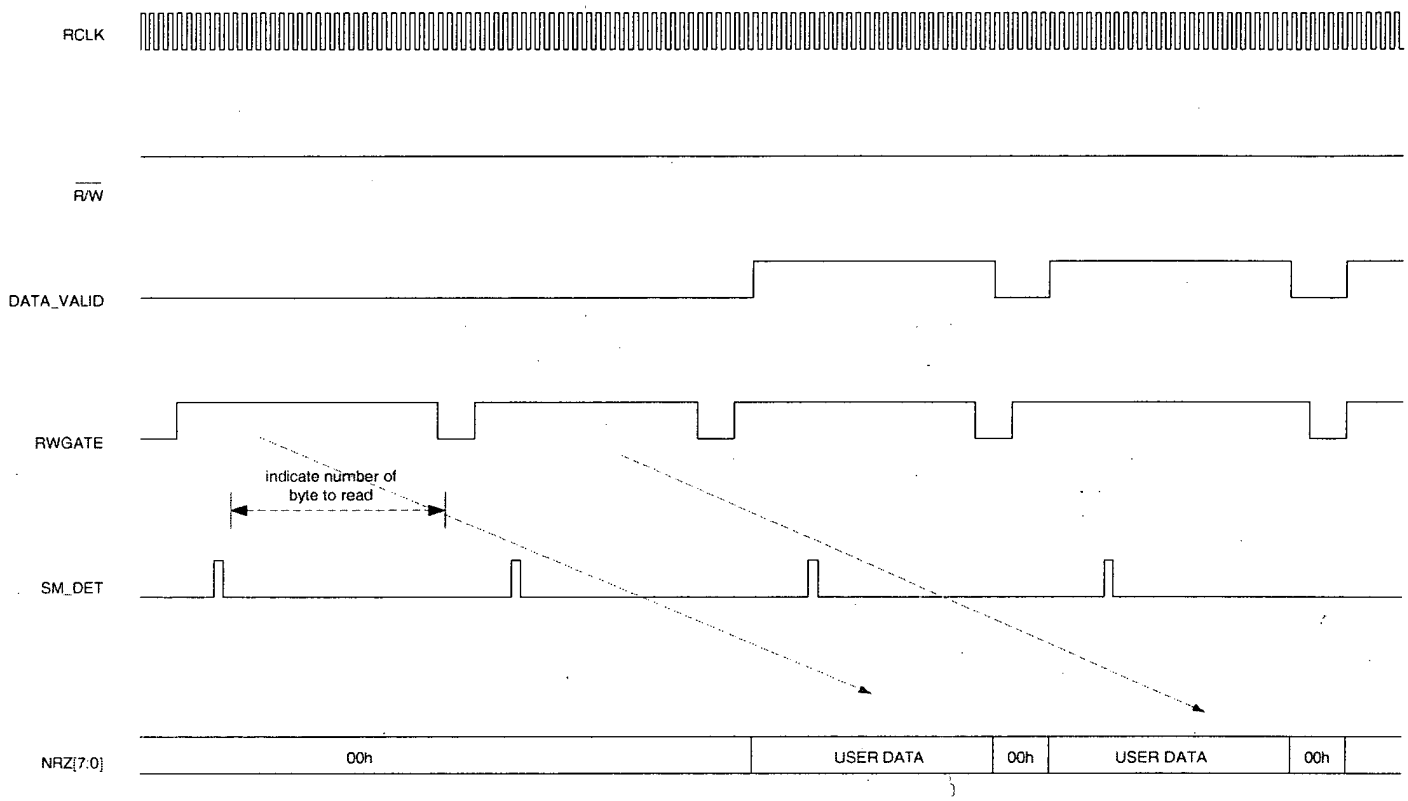
RCLK
R/W
DATA_VALID
RWGATE
indicate number of byte to read
SM_DET
NRZ[7:0]
00h
USER DATA
00h
USER DATA
00h

Fig. 30

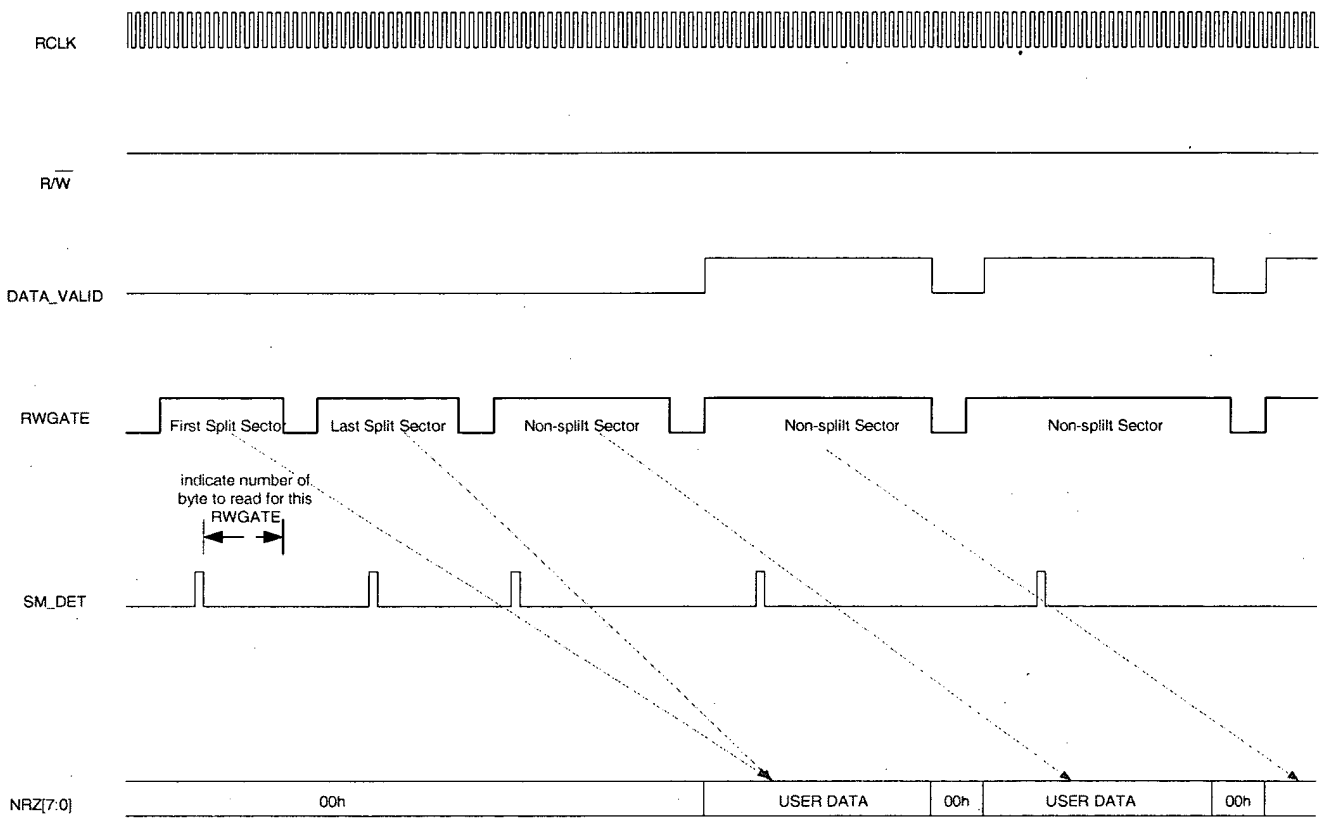
RCLK
R/W
DATA_VALID
RWGATE
First Split Sector
Last Split Sector
Non-splilt Sector
Non-splilt Sector
Non-splilt Sector
indicate number of byte to read for this RWGATE
SM_DET
NRZ[7:0]
00h
USER DATA
00h
USER DATA
00h

Fig. 31

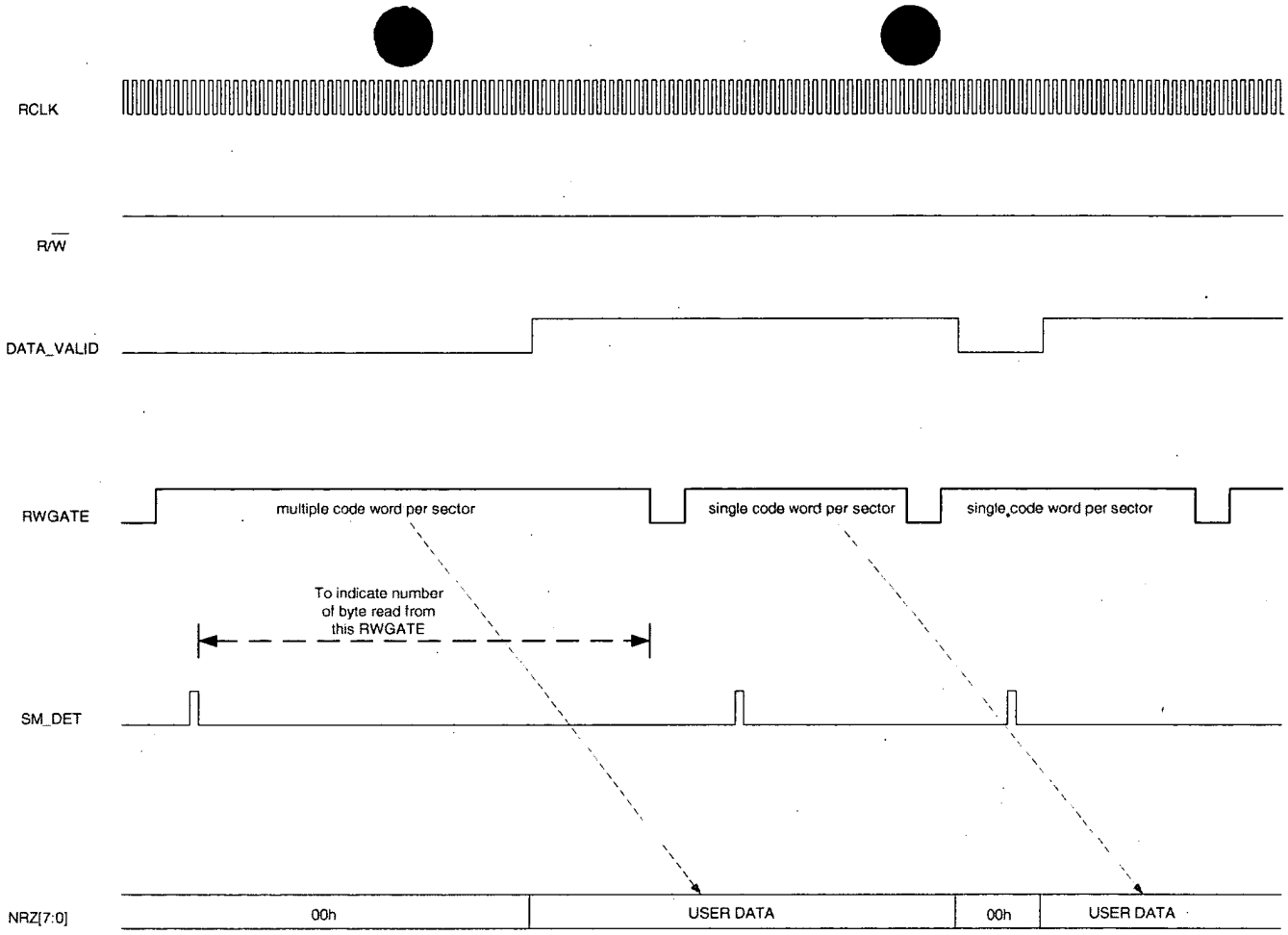
RCLK
R/W
DATA_VALID
RWGATE
multiple code word per sector
single code word per sector
single code word per sector
To indicate number
of byte read from
this RWGATE
SM_DET
NRZ[7:0]
00h
USER DATA
00h
USER DATA

Fig. 32

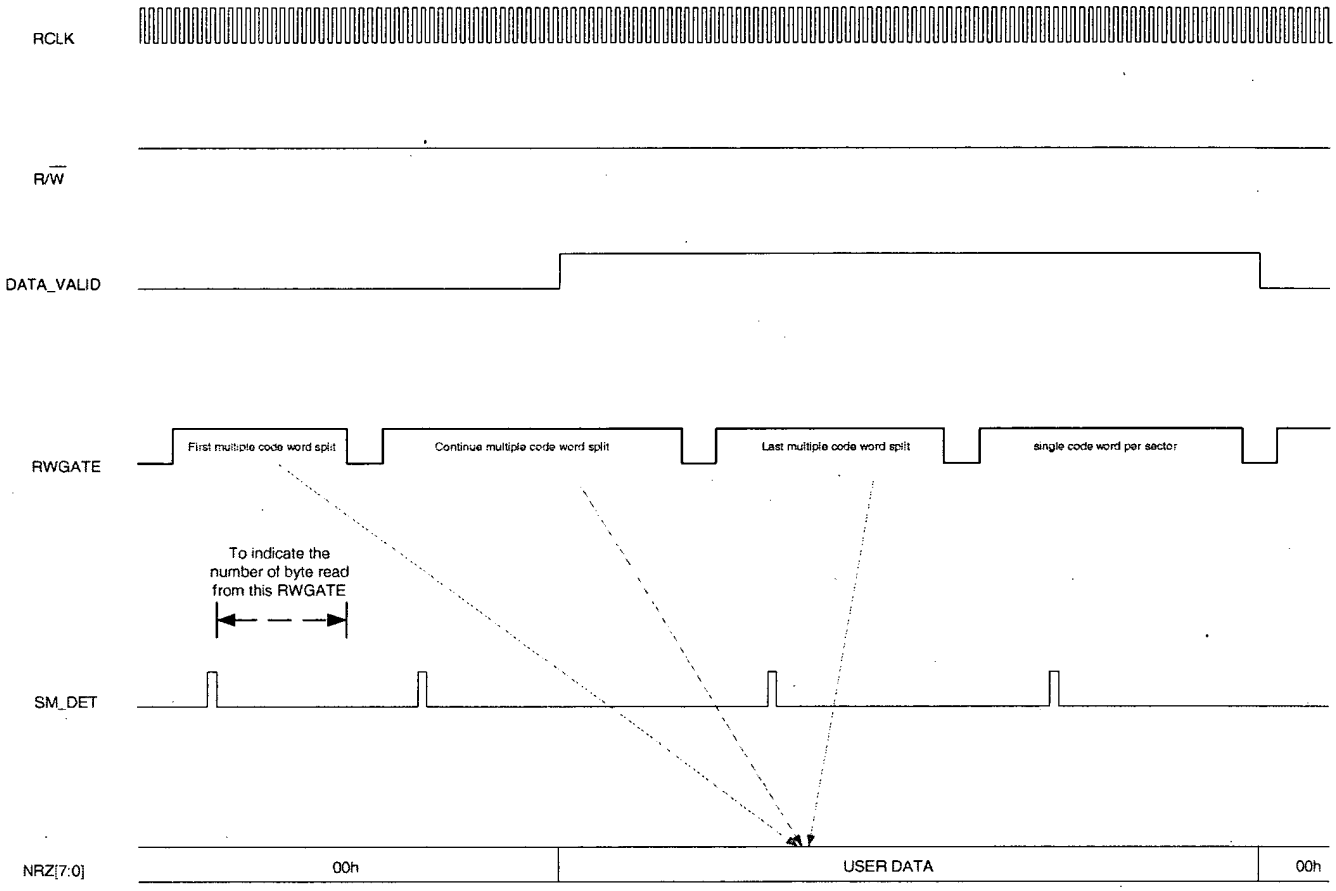
RCLK
R/W
DATA_VALID
RWGATE
First multiple code word split
Continue multiple code word split
Last multiple code word split
single code word per sector
To indicate the number of byte read from this RWGATE
SM_DET
NRZ[7:0]
00h
USER DATA
00h

Fig. 33

20'''

22'''

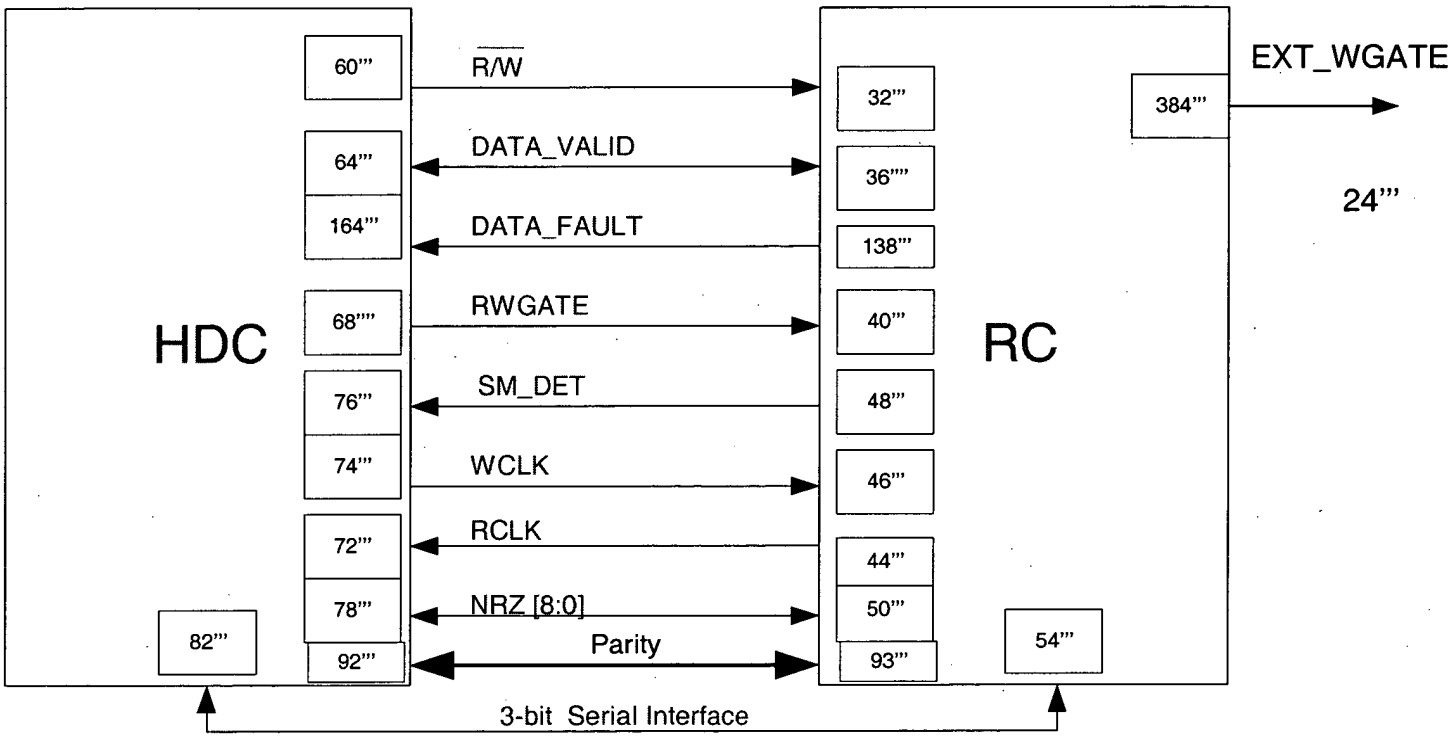
HDC
RC
60'''
64'''
164'''
68''''
76'''
74'''
72'''
78'''
82'''
92'''
R/W
DATA_VALID
DATA_FAULT
RWGATE
SM_DET
WCLK
RCLK
NRZ [8:0]
Parity
3-bit Serial Interface
32'''
36''''
138'''
40'''
48'''
46'''
44'''
50'''
93'''
54'''
384'''
EXT_WGATE
24'''

Fig. 34

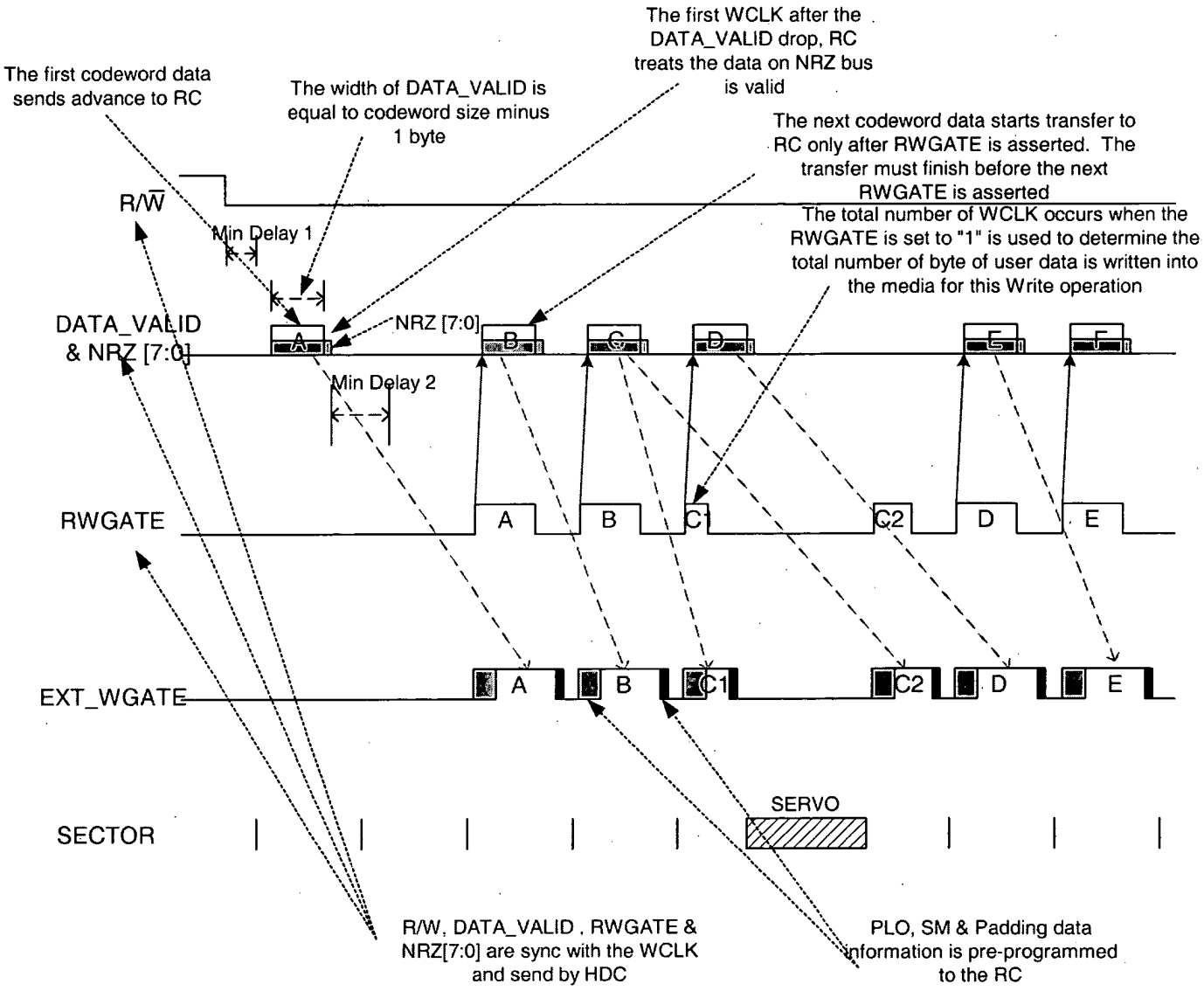
The first codeword data sends advance to RC
The width of DATA_VALID is equal to codeword size minus 1 byte
The first WCLK after the DATA_VALID drop, RC treats the data on NRZ bus is valid
The next codeword data starts transfer to RC only after RWGATE is asserted. The transfer must finish before the next RWGATE is asserted
The total number of WCLK occurs when the RWGATE is set to "1" is used to determine the total number of byte of user data is written into the media for this Write operation
R/W
Min Delay 1
DATA_VALID & NRZ [7:0]
NRZ [7:0]
Min Delay 2
RWGATE
EXT_WGATE
SECTOR
SERVO
A
B
C
D
E
F
C1
C2
R/W, DATA_VALID , RWGATE & NRZ[7:0] are sync with the WCLK and send by HDC
PLO, SM & Padding data information is pre-programmed to the RC

Fig. 35

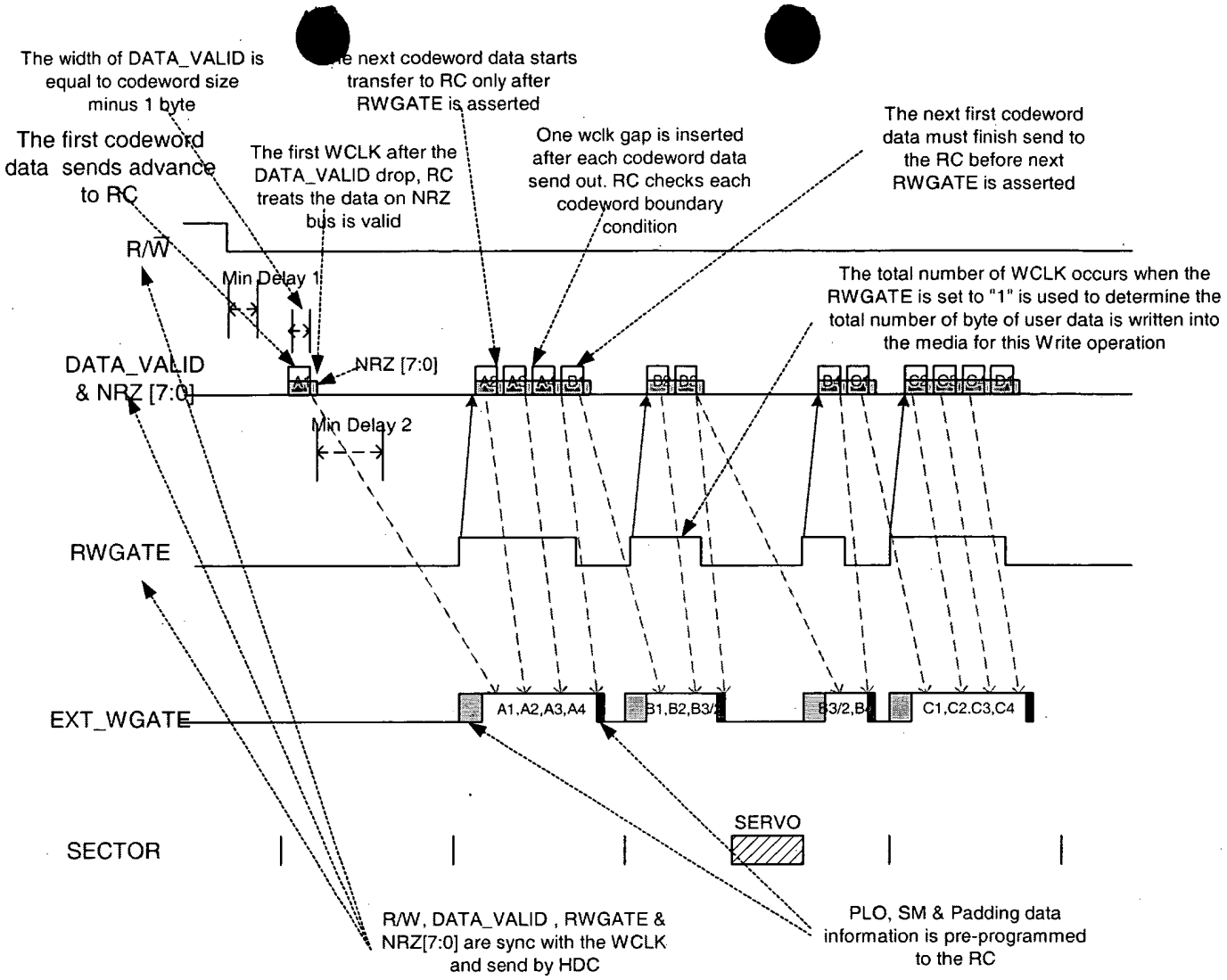
The width of DATA_VALID is equal to codeword size minus 1 byte
The next codeword data starts transfer to RC only after RWGATE is asserted
The first codeword data sends advance to RC
The first WCLK after the DATA_VALID drop, RC treats the data on NRZ bus is valid
One wclk gap is inserted after each codeword data send out. RC checks each codeword boundary condition
The next first codeword data must finish send to the RC before next RWGATE is asserted
R/W
Min Delay 1
The total number of WCLK occurs when the RWGATE is set to "1" is used to determine the total number of byte of user data is written into the media for this Write operation
DATA_VALID & NRZ [7:0]
NRZ [7:0]
Min Delay 2
RWGATE
EXT_WGATE
A1,A2,A3,A4
C1,C2.C3,C4
SERVO
SECTOR
R/W, DATA_VALID , RWGATE & NRZ[7:0] are sync with the WCLK and send by HDC
PLO, SM & Padding data information is pre-programmed to the RC

Fig. 36

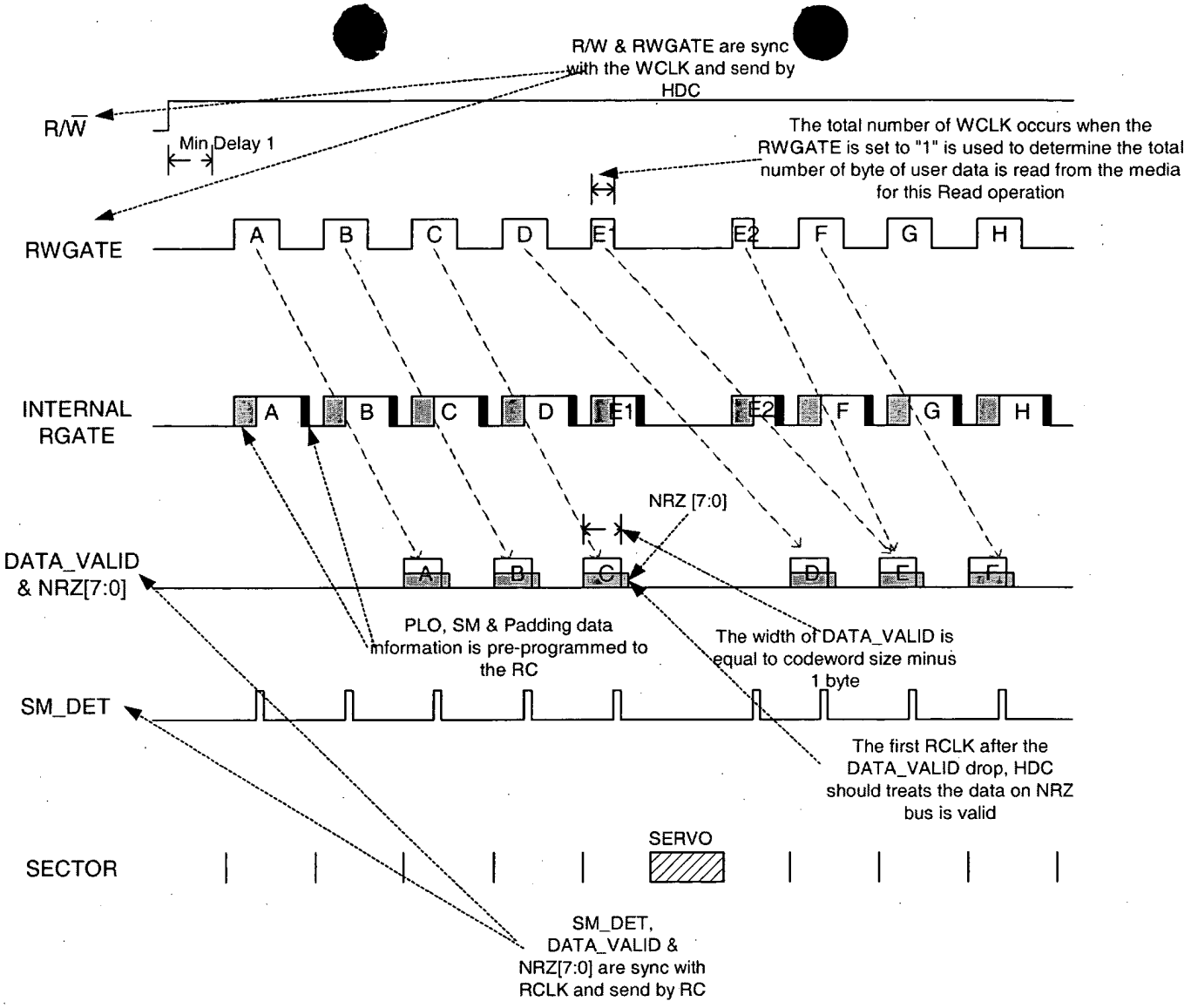
R/W & RWGATE are sync with the WCLK and send by HDC
R/W
Min Delay 1
The total number of WCLK occurs when the RWGATE is set to "1" is used to determine the total number of byte of user data is read from the media for this Read operation
RWGATE
A
B
C
D
E1
E2
F
G
H
INTERNAL RGATE
NRZ [7:0]
DATA_VALID & NRZ[7:0]
PLO, SM & Padding data information is pre-programmed to the RC
The width of DATA_VALID is equal to codeword size minus 1 byte
SM_DET
The first RCLK after the DATA_VALID drop, HDC should treats the data on NRZ bus is valid
SERVO
SECTOR
SM_DET, DATA_VALID & NRZ[7:0] are sync with RCLK and send by RC

Fig. 37

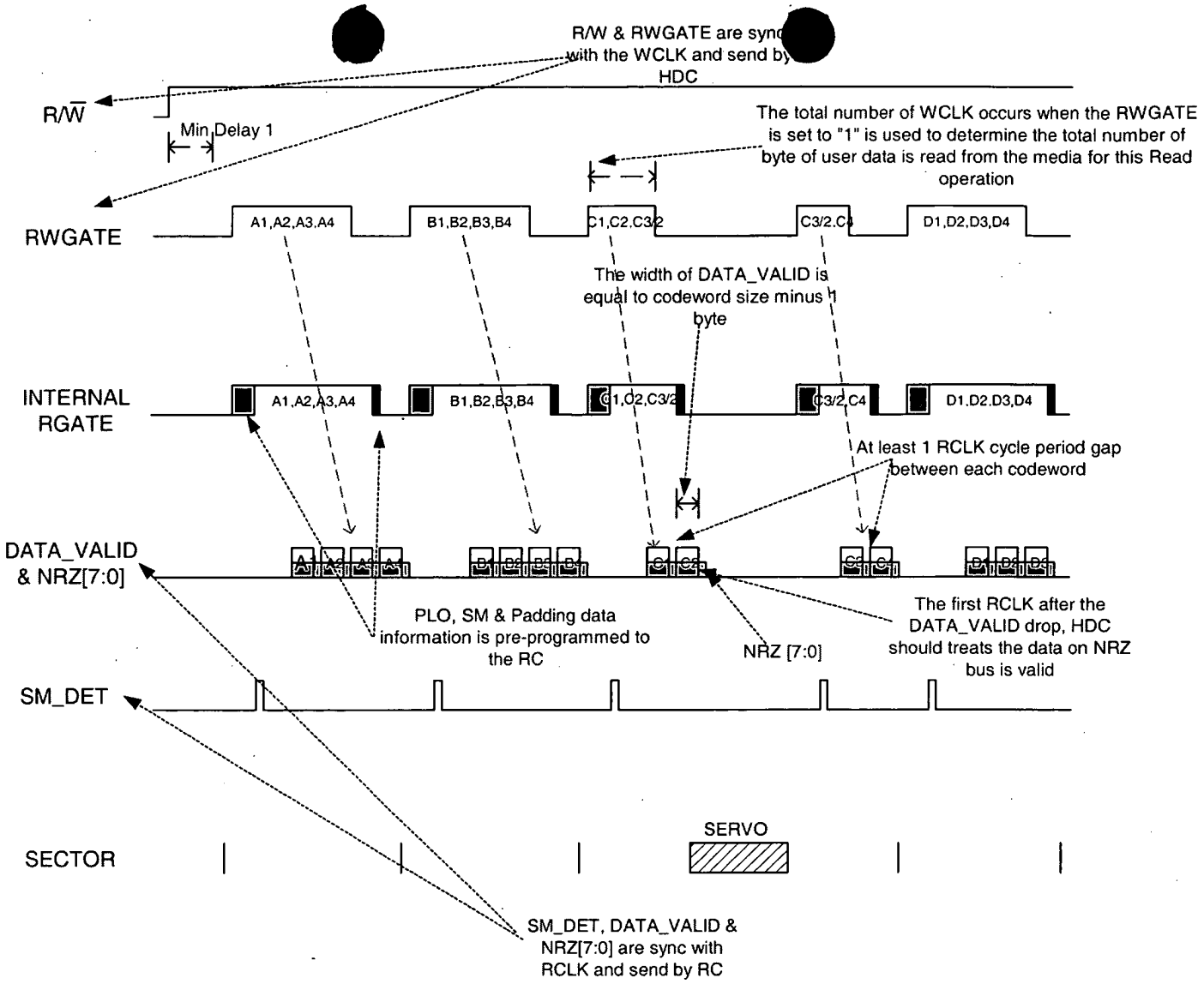
R/W & RWGATE are sync with the WCLK and send by HDC
R/W
Min Delay 1
The total number of WCLK occurs when the RWGATE is set to "1" is used to determine the total number of byte of user data is read from the media for this Read operation
RWGATE
A1,A2,A3,A4
B1,B2,B3,B4
C1,C2,C3/2
C3/2,C4
D1,D2,D3,D4
The width of DATA_VALID is equal to codeword size minus 1 byte
INTERNAL RGATE
At least 1 RCLK cycle period gap between each codeword
DATA_VALID & NRZ[7:0]
PLO, SM & Padding data information is pre-programmed to the RC
NRZ [7:0]
The first RCLK after the DATA_VALID drop, HDC should treats the data on NRZ bus is valid
SM_DET
SERVO
SECTOR
SM_DET, DATA_VALID & NRZ[7:0] are sync with RCLK and send by RC

Fig. 38